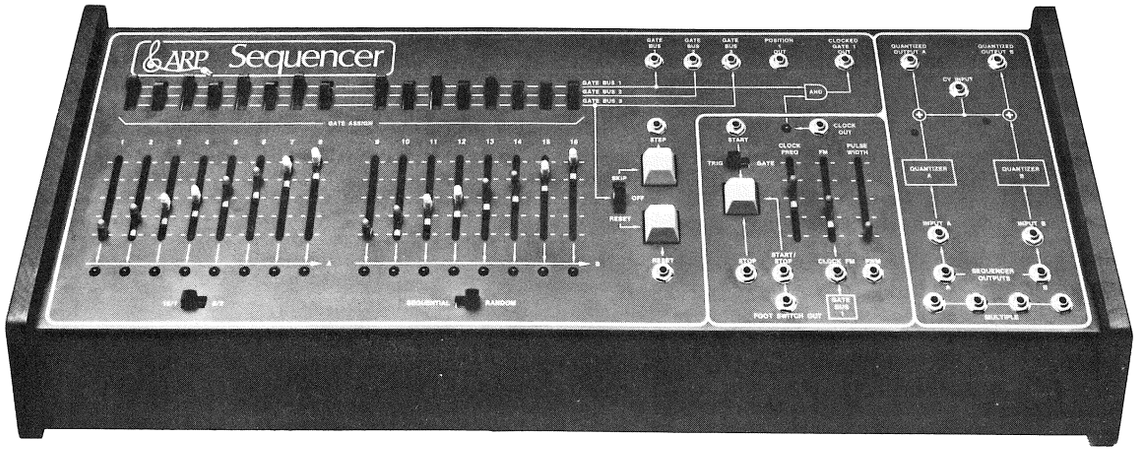
ARP SEQUENCER MODEL 1601

SERVICE MANUAL



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ARP SEQUENCER MODEL 1601

SERVICE MANUAL

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SECTION 1 INTRODUCTION

1.1 Product Description

The ARP Sequencer, model 1601, is a 16 step sequential voltage generator. A voltage level slider is provided for each of the 16 steps to adjust the voltage output from 0 to +10 volts. The sequencer may be used in a "8 X 2" mode so that outputs 1 through 8 (bank A) and 9 through 16 (bank B) sequence in parallel. The outputs of banks A and B are prewired to a voltage quantizer which effectively "rounds off" the sequencer's voltage to the nearest whole twelfth of a volt. This allows precise tuning since all ARP products are tuned to a 1 volt per octave standard (1/12 volt per semitone).

A low frequency voltage controlled clock governs the stepping speed of the sequencer and can be started, stopped, gated, or speeded up either manually or externally.

Position gates provide a constant voltage output (+10 volts) for as long as the sequencer is on a selected position. The position gate outputs are bused to one of the position gate outputs (Gate 1, 2, or 3).

1.2 Specifications

SEQUENCER

Number of positions 16

Maximum (unquantized) control voltage output . . . . . +12 V

Maximum Gate output voltage . . . . . +14 V

16 X 1 Mode . . Channels A and B are common

8 X 2 Mode . . . Channels A and B are separate

Step, Reset, Start, Stop and Start/Stop jack inputs . . . . . .Accepts +3 V to +10 V Gate

CLOCK

Type. . . . . .Voltage Controlled

Pulse Width . . . . . 10% to 100% (less 5 msec.)

PWM (Pulse Width Modulation) Input jack . . . . . .Accepts 0 to +10 volts

Frequency Range . . . . . 0.2 Hz. to 100 Hz.

FM Input Sensitivity . . . . . 2V/OCT max.

Clock Output . . . . . .+14 V pulse wave

Warm Up Drift 0

QUANTIZER

Function . . . . . ."Rounds off" voltages to nearest 1/12 V (semitone)

Maximum Input Voltage (A & B) . . . . . +10 V

Maximum Quantized CV Output (A & B) . . . . . +2 V

Range . . . . . 2 octaves

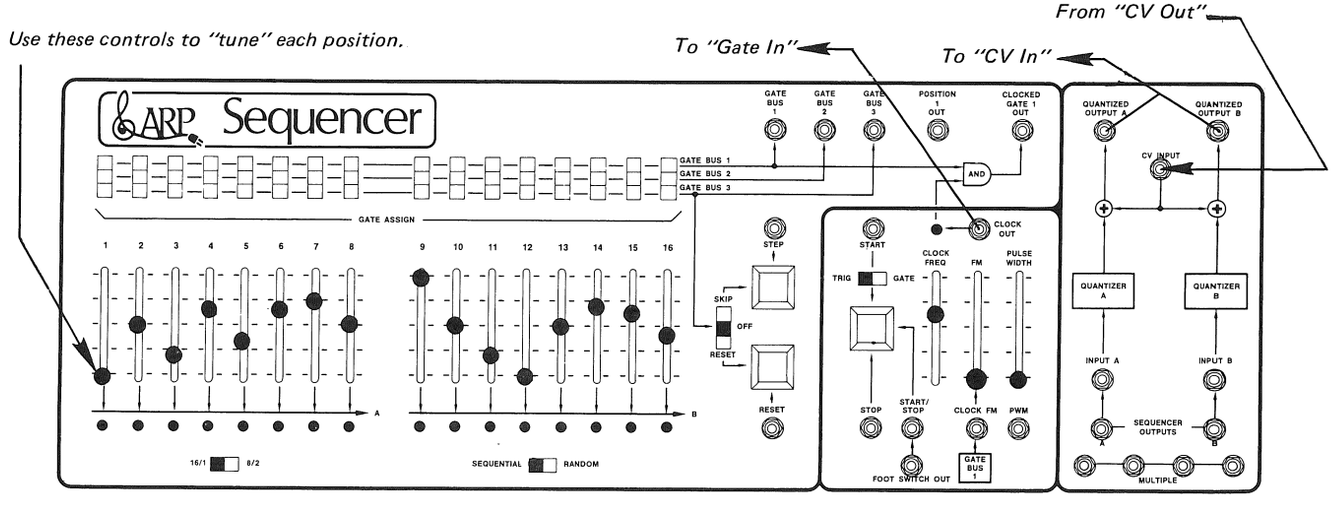
POWER REQUIREMENTS

Line Voltage. . . . . .100 to 130 VAC

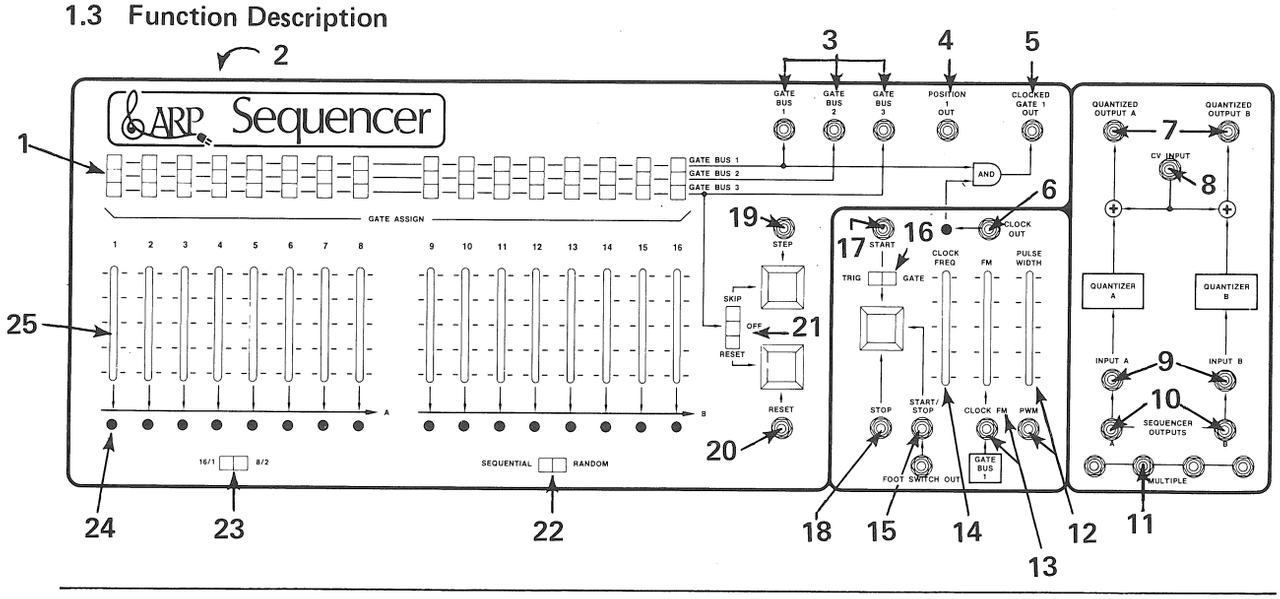
Line Frequency. . . . . .50-60 Hz.

Power . . . . . .20 Watts

FIG. 1.1 CONNECTIONS TO SYNTHESIZER



1.3 Function Description



1 *Position Gate Assignment Switches:* Supplies a +14 volt gate to one of three (bused) outputs.

2 *Foot Switch Input:* (Rear Panel) Supplies a +14 volt gate to the "Foot Switch Out" jack on the front panel.

3 *Position Gate Bus Outputs:*+14 volt gate outputs which are usually connected to external envelope generators.

4 *Position 1 Output:* Supplies a +14 volt gate on position 1 (only) to synchronize additional sequencers or synthesizers.

5 *Clocked Gate Out:* Allows the selection of particular position gates (Gate Bus 1) with control of the pulse width (Clock).

6 *Clock Out:* Supplies a +14 volt clock pulse which can trigger external envelope generators.

7 *Quantized CV Outputs:*Provides a control voltage in 1/12 volt increments (0 to +2 volt range) which controls the pitch of external oscillators. The A and B outputs are common in the 16 X 1 mode, but separate in the 8 X 2 mode.

8 *CV In:* Allows external control voltages (from a keyboard for example) to be summed with the sequencer's voltage to shift the key in which the sequencer plays.

9 *Quantizer Inputs:* Allows voltages to be "quantized" (rounded to nearest 1/12 volt). Prepatched to the sequencer outputs.

10 *Sequencer Outputs:* Provides a 0 to +10 volt analog control voltage.

11 *Common convenience jacks.*

12 *Pulse Width:* Varies the pulse width of the clock.

13 *Clock FM:* Allows external control voltages to increase the speed of the clock (prewired to Gate Bus 1).

14 *Clock Frequency:* Manually varies the clock rate from .2Hz to approx. 100 Hz.

15 *Start/Stop:* Alternately starts and stops the sequencer.

16 *Trig/Gate Switch:* Trigger mode allows the sequencer to be "triggered" on. In the Gate mode, the sequencer is on while the start button is held.

17 *Externally starts the sequencer.*

18 *Externally stops the sequencer.*

19 *Step:* Advances the sequencer to the next position.

20 *Reset:* Resets the sequencer to position 1 (sequential mode only).

21 *Skip/Reset:* Allows particular positions (from gate bus 3) to either skip past or reset on particular positions.

22 *Sequential/Random Mode:* Allows clock to advance to each successive position or advance to a random position.

23 *Mode Switch:* Steps the sequencer 16 times, or steps banks A and B 8 times in parallel.

24 *LEDs:* (Light Emitting Diodes) Indicates which position is on.

25 *Position Tuning Sliders:* Tunes individual positions (adjusts CV level).

SECTION 2 THEORY OF OPERATION

2.1 Sequencer

The heart of the sequencer is the Counter/Latch circuit which produces a four bit binary number. When initially reset, the output of the counter is 0000 (Position 1 code), or zero. Each time the counter receives a pulse from the Mask circuit, the counter advances to the next binary number (0001, 0010, 0011, 0100...1111). The highest binary number, 1111, corresponds to position 16.

This code is supplied to the Decoder circuit which decodes the binary number to one of 16 outputs. For example, when the code 0000 is present on the output of the counter, the decoder will turn on the position 1 output (only); when the code 0001 is present on the output of the counter, the decoder will turn on only the position 2 output, etc.

When in the "8 X 2" mode, a three bit code is supplied from the counter instead of four. Positions 1 through 8 and 9 through 16 in the Decoder circuit simultaneously decode so that bank A (1-8) and B (9-16) sequence in parallel.

The Voltage Controlled Low Frequency Clock determines when the counter is advanced to the next position by pulsing a one shot circuit. The one shot in turn supplies a pulse to the Mask circuit which advances the counter and disables (masks) the gate outputs during the count advance.

When the sequencer is in the random mode, the Randomizer circuit advances the counter at an extremely high frequency. For each cycle of the low frequency clock, a position number on the output of the counter is memorized and held until the next clock pulse. Since the counter is being advanced so fast, the position numbers which are memorized will be random.

2.2 Quantizer

Voltages which are to be quantized to the nearest whole twelfth of a volt are applied to the "A" or "B" input of the quantizer. One quantizer circuit is multiplexed by switching between one of the two inputs (A and B) to provide two independent quantized control voltage outputs. The voltages are quantized and stored extremely quickly, so that two different voltages are quantized (one at a time) faster than can be detected by the ear. As in a standard keyboard, a resistor chain of equal value resistors make up a voltage divider to generate a voltage reference. The voltages produced by this reference CV generator are 0 volts, 1/12V, 2/12V, 3/12V...2V (2 octave range). A high frequency oscillator steps a counter which enables the CV generator voltages to be "scanned" one at a time (0 volts to 2 volts).

The input voltage which is to be "quantized" is compared to the reference CV on the scanner output; if the scanner output is lower than the input voltage, the counter advances until the scanner voltage is just higher than the input voltage. The counter is then stopped (by the Comparator circuit) and the voltage on the output of the scanner is memorized. The counter is then reset to zero so that the voltage on other input may be quantized next.

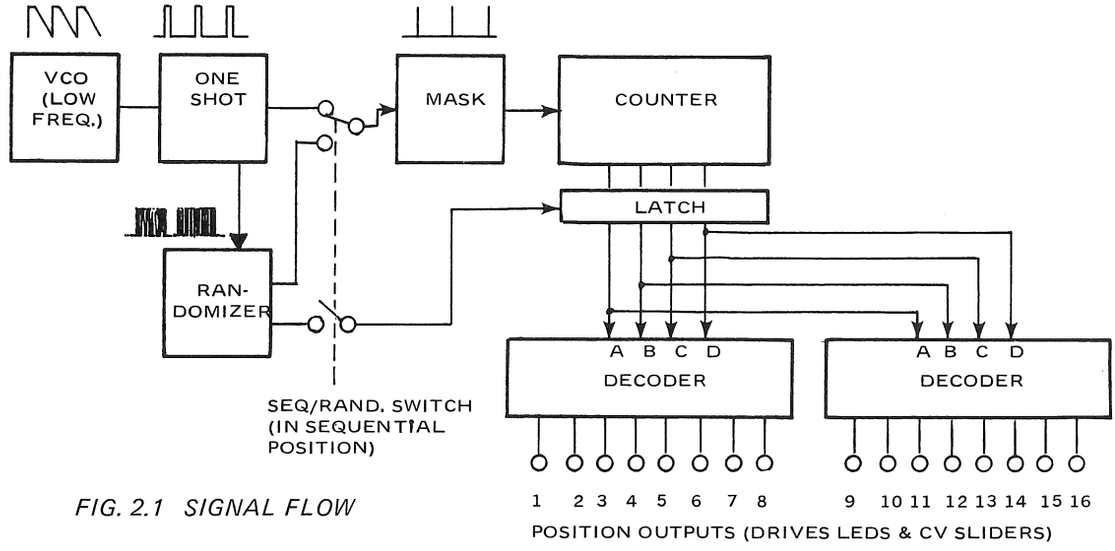


FIG. 2.1 SIGNAL FLOW

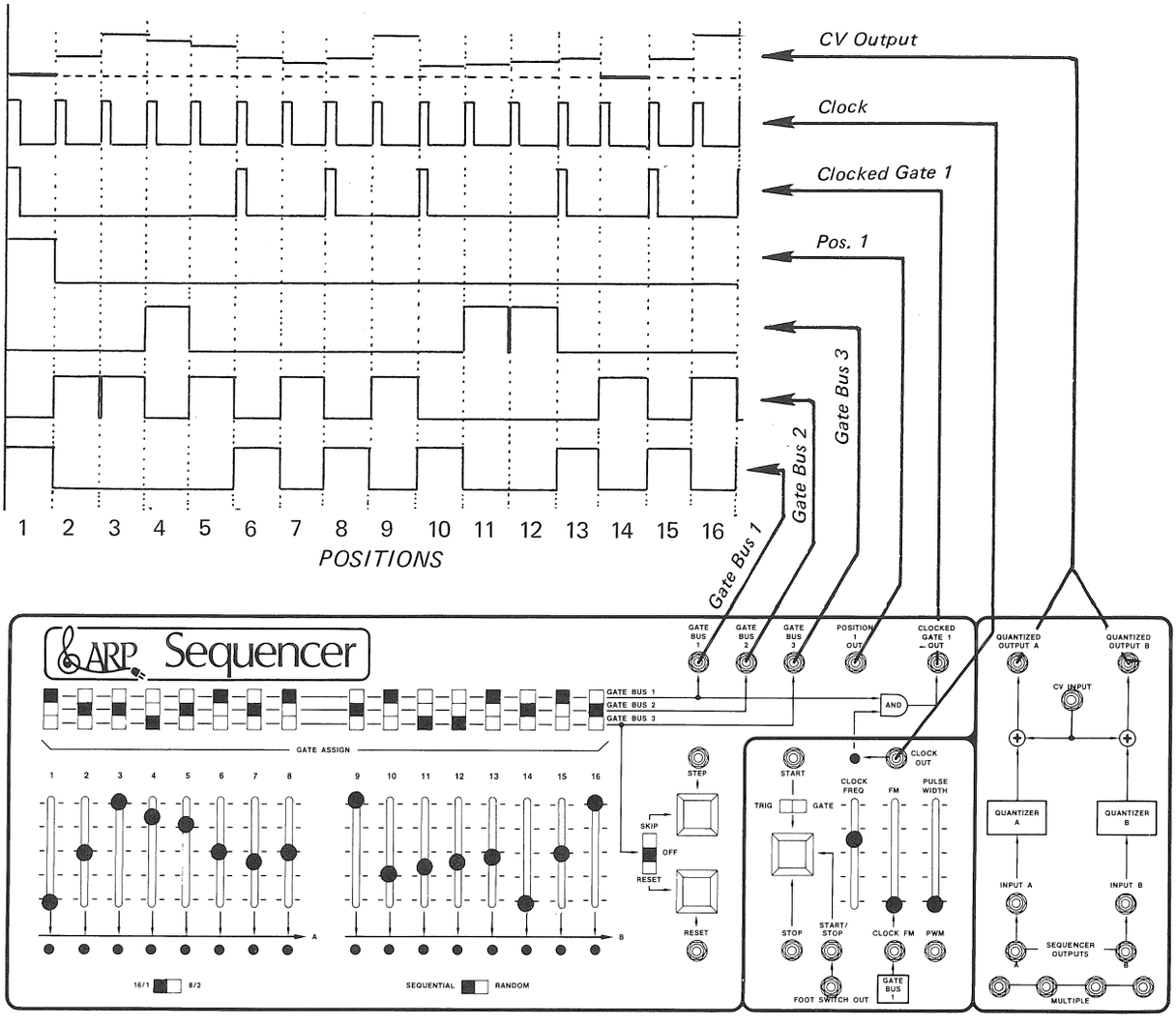


FIG. 2.2 SEQUENCER OUTPUTS

SECTION 3 CIRCUIT DESCRIPTIONS

3.1 Clock On/Off

Gate signals applied to the start jack set the Q output of Z2B to logic 1 (+15 volts) and Q bar to logic 0 (0 volts). Gate signals applied to the stop jack set the Q output of Z2B to logic 0 and the Q bar to logic 1. Each time a gate signal is applied to the start/stop jack or when the start/stop button is depressed, the Q output of Z2B assumes the logic level of the Q bar output so that the Q and Q bar outputs reverse state.

When the Gate/Trigger switch (S2) is in the gate position, the Q output will assume a logic 1 state for as long as a gate is present on the start/stop jack.

Summary: For a clock "on" state, the Q output of Z2B (B point) will be a logic 1. For a clock "off" state, the Q output is a logic 0.

3.2 One Shot

A 4 millisecond pulse occurs on the Q output of Z11A when pulsed on the A input (pin 5). The pulse on the output of the one shot is supplied to: 1) the Clock Oscillator to reset the sawtooth: 2) the Reset circuit to lengthen the external reset pulse (if applied) when the E point is at a logic 1; and 3) the Randomizer circuit to momentarily disable the high frequency oscillator (random mode only).

3.3 Clock Oscillator

Three circuits comprise the Clock Oscillator: the Voltage Controlled Oscillator, Sawtooth to Pulse Converter, and Comparator.

Sawtooth Oscillator: Voltages from the clock FM input jack and the clock rate slider are summed on

the base of Q4. Q4 and Q5 are a linear voltage to exponential current converter. Capacitor C7 is initially charged to +15 volts and discharges toward ground through Q5. Z3A and Q7 follow the voltage level on C7 and supply it to the comparator and the sawtooth to pulse converter. The output of the comparator (pin 13, 8) will switch to +15 volts (logic 1) when the sawtooth voltage falls below +7.5 volts. The comparator output is supplied to the one shot which reset capacitor C7 to +15 volts.

Sawtooth To Pulse Converter: Voltages from the Pulse Width Modulation jack and the Pulse Width slider are applied to Z4A and Z4B to set the clock pulse width. The collector of Q8 will be a pulse wave with a pulse width from 20% to 100% depending on the position of the pulse width slider. The pulse output of the clock oscillator is routed to the Gate Output Processing circuit (schematic 2).

3.4 Randomizer, Skip & Reset

Z11B is a high speed oscillator (approx. 5 microsec.). When Z16A pin 3 is a logic 1, Z11B produces a high frequency pulse chain on pin 9. When Z16Z pin 3 is at a logic 0 (ground) Z11B stops oscillating. With slide switch S21 in the Random position, Z10C pin 10 will enable (turn on) the high speed oscillator (Z11B) through Z16A. Z11B will then provide a pulse chain to Mask circuit. When pulsed by the clock oscillator, the one shot will momentarily turn off the high speed oscillator through Z10C (pin 12 & 13) to allow the latch in the Counter/Latch circuit to memorize a (random) position. During this mode, Z7B generates random voltage levels to vary the frequency of Z11B to insure a random sampling of positions. With S21 in the Sequential mode, Z10C will not affect the frequency of the high speed oscillator. When S22 is in the skip position, pin 8 of Z9C is at logic 0. When the J point is also at a logic 0, Z9C pin 10 then turns on the high speed oscillator which quickly advances the sequencer to the next position (via Z16C).

In the reset position, the gate signal on the J point is supplied through S22 to Z9D. When the J point is at logic 0, Z9D supplies a logic 1 which resets the counter to position 1 via Z16B. External reset gates may be applied to Q27 and by depressing the reset push button (S23).

3.5 Mask Circuit

Z15A pin 3 is logic 1 when the sequencer is in the "sequential" mode which allows the latch (Z8) in the Counter/Latch circuit to transmit data continuously. When pin 3 of Z15A is logic 0, (random mode only) Z8 in the Counter/Latch circuit holds or stores the data on the counter output.

The one shot pulse will cause the Q and Q bar outputs of Z2A to momentarily reverse state. The output of the high speed oscillator (Z11B) and the Q bar output of Z2A are then combined on Z16C which advances the counter in the Counter/Latch circuit. A "mask" pulse is generated by combining the one shot pulse (4 msec. duration) and the pulse from Z2A (8 microsec. duration) on the output of Z15B (pin 4) to turn off all the gate outputs during the time the counter is advanced from one position to the next.

3.6 Step

When gate signals are applied to the step jack or from the step push button, Z6A pin 3 provides a pulse to the One Shot circuit and the Gate Output Processing circuit.

3.7 Foot Switch Jack

The foot switch jack on the front panel provides a +10 volts gate for as long as the foot switch is held and can be patched to any of the input jacks on the front panel.

3.8 Counter/Latch

Z7A is a divide by 16 counter providing a 4 bit code to Z8. Z8 is a latch circuit but normally transmits data to the Decoder circuit unaffected. Z9B and Z9A are connected to the Q and Q bar outputs of Z8 to enable Z13 and Z14 in the Decoder circuit one at a time (sequentially).

3.9 Decoder

Z13 and Z14 decode the binary number from the Latch circuit to one of 16 positions. When S4B is in the 16 X 1 mode, Q11 through 26 will turn on one at a time sequentially (1 through 16). In the 8 X 2 mode, Z13 and Z14 decode in parallel (position 1-8 and 9-16). In the random mode, the counter advances at the rate of the High Speed Oscillator (Z11B, schematic 1) but in this mode, Z8 holds the code which is supplied to the decoders constant. The strobe input of the Z8 allows a random binary number to be memorized on each clock pulse which is supplied to the decoder.

Q11 and Q26 are turned on one at a time and supply voltages to one of the three gate bus lines through the three position gate switches. At the same time, the LED is lit indicating which position is on. The three position slide switches provide the path to ground for the LEDs.

The voltages from the decoder chips are also supplied to 100K sliders (R57 through R103) to provide a variable voltage level (0 to +10V) for each position.

Voltages from the A bank sliders and the B bank sliders are summed in the output amplifier circuit Z19A and Z18A. When the sequencer is in the 16 X 1 position, the output of the A and B channels are summed together so that the outputs of Z19B and Z18B will be the same. The Sequencer output voltages supplied by the output amplifiers are routed to the quantizer (schematic 3).

3.10 Gate Output Processing

Gate Output Processing circuit provides 6 outputs: Gate Bus 1, Gate Bus 2, Gate Bus 3, Clocked Gate 1, Clock Output, and Position 1 Output.

The Gate Bus 1, 2, and 3 outputs are driven from the 3 position slide switches in the Decoder circuit. Z15C and Z15D are a flip-flop which supplies the Clocked Gate 1 Output and turns on the clock indicator light (CR22). The position 1 output obtains its signal from Position 1 (Q11 base) in the Decoder circuit so that more than one sequencer can be synchronized.

QUANTIZER

3.11 Current Source & Semitone Shift

Z29A supplies constant current through 13 equal value resistors (100ohm) located in resistor pack Z20. The voltage drop across each resistor is 2/12 of a volt (two semitones, or one whole tone). Q36 supplies an offset voltage to pin 3 of Z29A to "shift" or raise the output of the current source (and therefore pins 1 through 14 of Z20) up 1/12 of a volt.

3.12 CV Generator & Scanner

Z21 and Z22 are digitally controlled analog switches which are connected to the CV generator outputs (Z20). The three binary inputs (A, B and C) select one of eight switches to be turned on and connect an input (pins 13, 14, 15, 12, 1, 5, 2, or 4) to the output (pin 3). All of the switches are off when a logic 1 is on pin 6 (inhibit). The A, B and C inputs of Z21 are driven by Z25.

3.13 COUNTER

Z25 generates a binary number which "counts" from 00000 to 11111. The first bit (MSB) inhibits either Z21 or Z22 so that only one voltage from Z20 is ever on at the same time. The next three bits (pins 6, 9, and 11 of Z20) turn on channels 13, 14, 15, 12, 1 etc. one at a time sequentially. The remaining bit (LSB) on the Counter output (pin 12) is supplied to the Current Source to shift the resistor chain level up 1/12 of a volt to obtain two voltage levels per resistor in Z20.

3.14 Comparator

The scanner output (Z29B pin 7) is supplied to the inverting input of the Comparator (Z23). An external control voltage which is to be quantized is supplied to the noninverting input of the Comparator via the Input Channel Selector.

Initially, the Comparator output is logic 1 (+15 volts) which permits the counter to be advanced by the Clock through Z24D. As the Counter advances, the voltage on pin 2 of Z23 "steps" in 1/12 volt increments until it exceeds the voltage level on pin 3 of Z23. The output of the Comparator then changes to logic 0 which immediately stops the Counter. The voltage on the Scanner output (now constant) is the nearest 1/12 of a volt level to the input control voltage; therefore, it is supplied to the Channel Memory via Z30C to be stored.

3.15 Sample Control

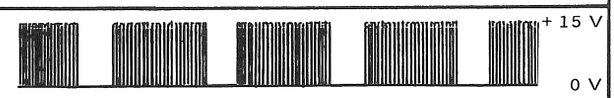
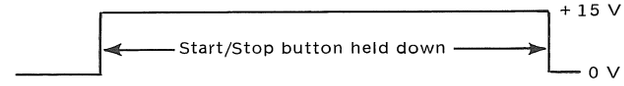
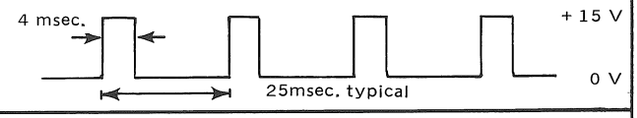
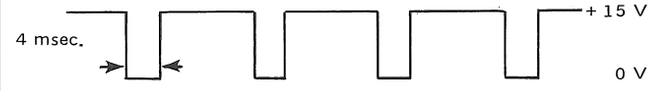
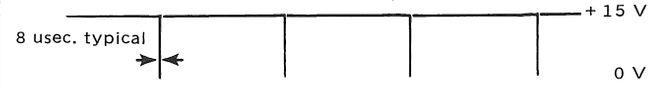
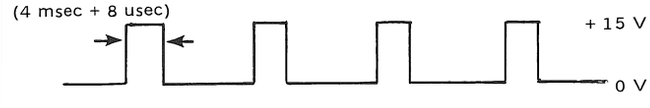
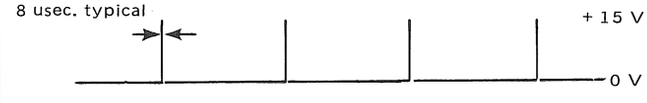
Z30C is enabled when the Sample Control provides a logic 1 to the clock input of Z28A. Z28A then turns on one of the transmission gates (either channel A or B) for a time period of half a clock cycle. After the quantized control voltage from Z29C has been supplied to one of the memory circuits, Z27C resets both the Sample Control and the Counter. Additionally, the outputs of Z28A reverse state to switch from one channel to the other (A to B for example). The Quantizer is now ready to quantize the voltage waiting on the other input.

3.16 External CV Input

The External CV input allows a control voltage from another synthesizer to be summed with the output of the two Quantizer circuits. The keyboard CV of other instruments can be added to the sequencer's voltage to change the key in which the sequencer plays simply by playing an external keyboard.

The test points on the following two pages illustrate the operation of the circuits in the sequencer in relation to one another.

SECTION 4 SEQUENCER TEST POINTS

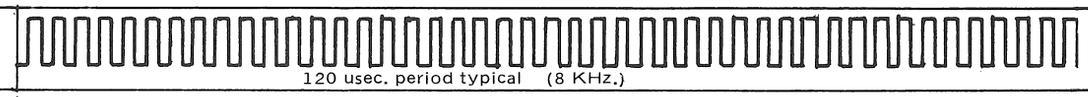
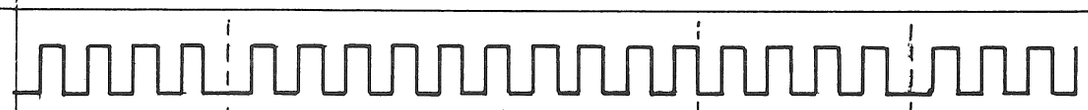
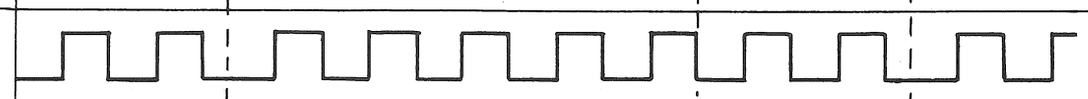
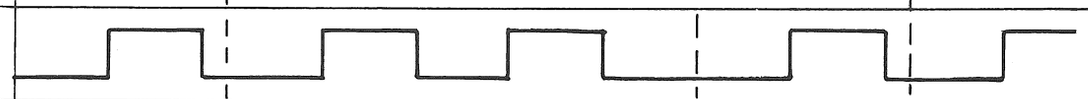
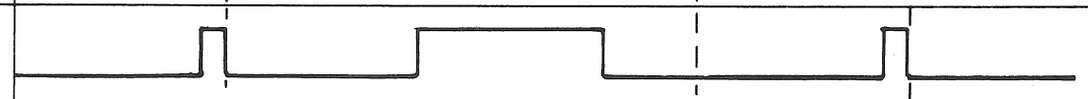
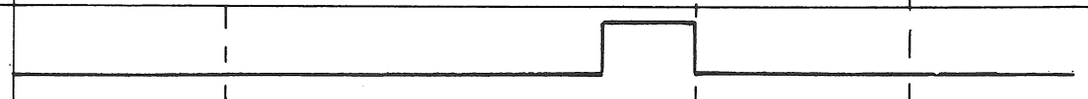
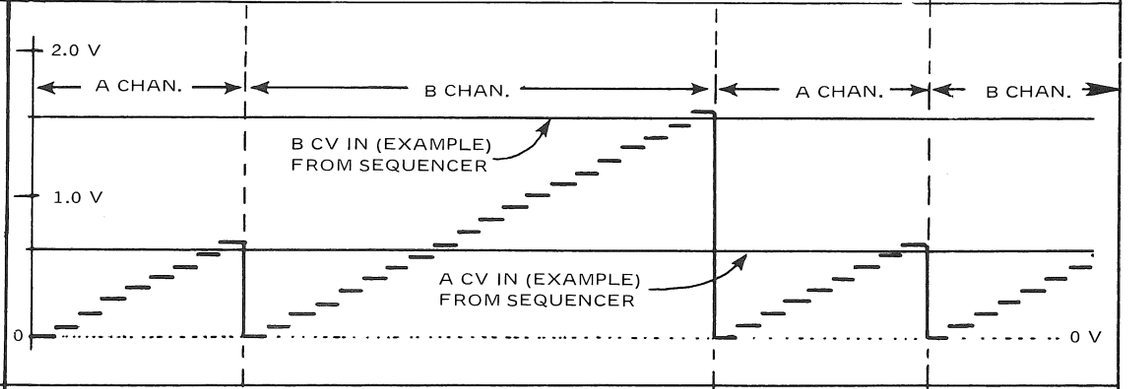
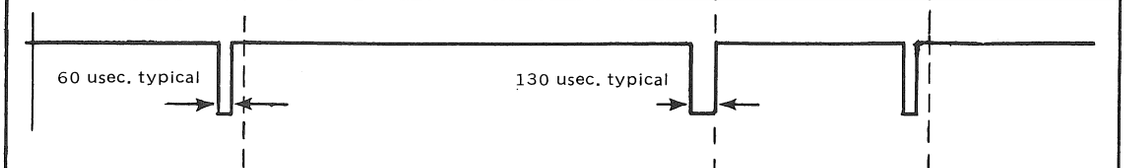
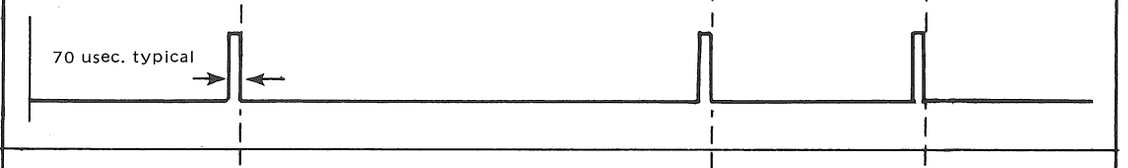
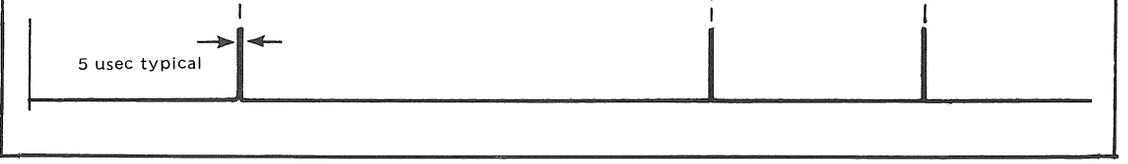
TEST POINT	FUNCTION	SET UP	SPECIFICATIONS
TP-1	HIGH FREQ. OSC.	1. Put the SEQ/RAND switch in the RANDOM mode.	
		2. Put the SEQ/RAND switch in the SEQUENTIAL mode.	0 volts (constant)
TP-2	CLOCK ON/OFF	1. Put the TRIG/GATE switch in the GATE position. Depress the START/STOP button.	
		2. Put the TRIG/GATE switch in the TRIGGER position. Depress the START/STOP button.	Alternates between +15 V and 0 V when START/STOP is depressed.
TP-3	ONE SHOT	1. Put the CLOCK FREQ. slider at ¾. 2. Put all other sliders fully DOWN. 3. Start the Sequencer.	
TP-4	CLOCK SAWTOOTH	1. Put the CLOCK FREQ. slider at ¾. 2. Put all other sliders fully DOWN. 3. Start the Sequencer.	
TP-5	COMPAR-ATOR	1. Put the CLOCK FREQ. slider at ¾. 2. Put all other sliders fully DOWN. 3. Start the Sequencer.	
TP-6	CLOCK	1. Put the CLOCK FREQ. slider at ¾. 2. Put all other sliders fully DOWN. 3. Start the Sequencer.	
		4. Put the PULSE WIDTH slider fully up.	+15 volts (constant)
TP-7	$\overline{\text{ONE SHOT}}$	1. Put the CLOCK FREQ. slider at ¾. 2. Put all other sliders fully DOWN. 3. Start the Sequencer.	
TP-8	MASK ADVANCE	1. Put the CLOCK FREQ. slider at ¾. 2. Put all other sliders fully DOWN. 3. Start the Sequencer.	
TP-9	MASK	1. Put the CLOCK FREQ. slider at ¾. 2. Put all other sliders fully DOWN. 3. Start the Sequencer.	
TP-10	ADVANCE	1. Put the CLOCK FREQ. slider at ¾. 2. Put all other sliders fully DOWN. 3. Start the Sequencer.	

The following test points all use the same panel settings:

NOTE: Test points 11-17 and 19-20 are +15 V pulse waves.

QUANTIZER

1. Put the SEQ/RAND switch in the SEQUENTIAL position.
2. Put the GATE/TRIG switch in the GATE position.
3. Put the mode switch in the 8 X 2 position.
4. Depress the RESET button (position 1 LED should be lit).
5. Put the POSITION 1 slider about 1/3 up.
6. Put the POSITION 9 slider about 2/3 up.

TEST POINT	FUNCTION	SPECIFICATIONS
TP-11	Ø 2 CLOCK	
TP-12	Ø 1 CLOCK	
TP-13	SEM. SHIFT	
TP-14	SCANNER A	
TP-15	SCANNER B	
TP-16	SCANNER C	
TP-17	SCANNER I	
TP-18	SCANNER OUTPUT	
TP-19	COMPAR-ATOR	
TP-20	SAMPLE	
TP-21	RESET	

SECTION 5 CALIBRATIONS

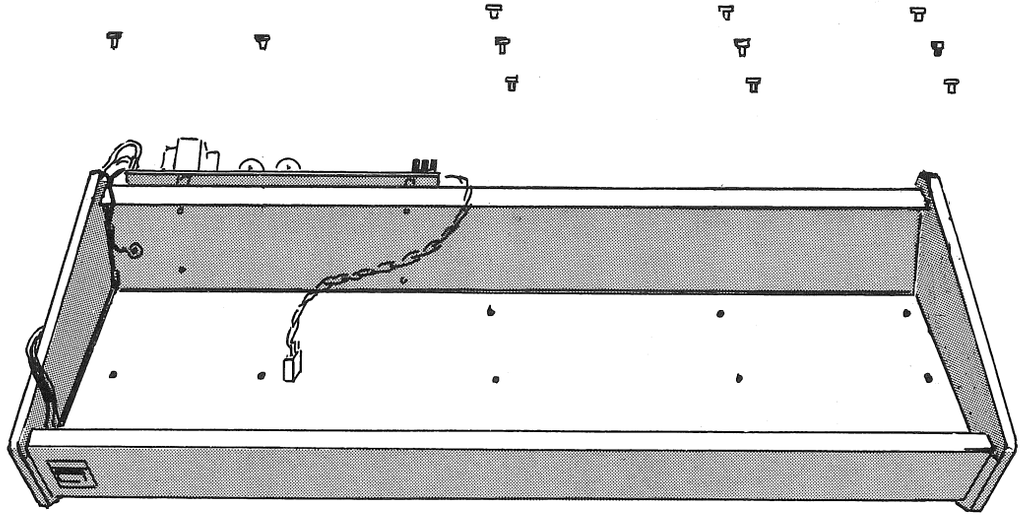
5.1 Sequencer & Quantizer

REF. NO.	TRIMMER.	TRIM PROCEDURE
R19	FREQ. CAL.	1. Put the CLOCK FREQUENCY SLIDER fully UP. 2. Monitor the CLOCK OUTPUT with a frequency counter or oscilloscope. 3. Put all other sliders fully DOWN. 4. Adjust trimmer R19 for a 10 msec. period waveform (100Hz.).
R26	PULSE WIDTH	1. Put all GATE ASSIGNMENT switches fully UP (Gate Bus 1 position). 2. Monitor the CLOCKED GATE 1 OUTPUT with an oscilloscope. 3. Put the GATE/TRIG switch in the TRIGGER mode. 4. Depress the START/STOP button to START the sequencer. 5. Put the CLOCK FREQUENCY slider fully UP. 6. Put the CLOCK FM slider fully DOWN. 7. Put the CLOCK PULSE WIDTH slider fully UP. 8. Turn trimmer R26 fully CLOCKWISE. 9. SLOWLY turn trimmer R26 COUNTER CLOCKWISE until waveform disappears (constant +14 volts). TURN NO FURTHER.
R206 & R207	A OFFSET & B OFFSET ADJUST	1. Connect a patch cord from INPUT A jack to INPUT B jack (isolates quantizer inputs). 2. Adjust trimmer R206 for 0 volts ±.005 V on QUANTIZED A OUTPUT. 3. Adjust trimmer R207 for 0 volts ±.005 V on QUANTIZED B OUTPUT.
R226 & R222	QUANTIZER CV V/OCT	1. Put all sliders on the sequencer fully DOWN. 2. Put the TRIG/GATE switch in the GATE mode. 3. Put the sequencer mode switch in the 16 X 1 POSITION. 4. Put the SEQ/RAND switch in the SEQUENTIAL position. 5. Depress the RESET button (position 1 LED should be lit). 6. Put the POSITION 1 SLIDER fully UP. 7. Adjust trimmer R266 for +2.00 volts on the QUANTIZED OUTPUT A jack. 8. Adjust trimmer R222 for +2.00 volts on the QUANTIZED OUTPUT B jack.
R217 & R218	A MOD ADJUST B MOD ADJUST	1. Put all the sliders on the sequencer fully DOWN. 2. Put the GATE/TRIG switch in the GATE mode. 3. Put the mode switch in the 16 X 1 POSITION. 4. Put the SEQ/RAND switch in the SEQUENTIAL position. 5. Depress the RESET button (position 1 LED should be lit). 6. Connect a patch cord from INPUT A jack to INPUT B jack (isolates quantizer inputs). 7. Monitor the A SEQUENCER OUTPUT with a DVM. 8. Raise the POSITION 1 SLIDER to ½. 9. Measure and record the EXACT VOLTAGE level on the A sequencer output (should be near +5 volts). 10. Connect a patch cord from the A SEQUENCER OUTPUT jack to the CV IN jack. 11. Monitor the QUANTIZER OUTPUT A with a DVM. 12. Adjust trimmer R217 for EXACTLY the same voltage as measured in step 9 (unity gain). 13. Monitor the QUANTIZED OUTPUT B with a DVM. 14. Adjust trimmer R218 for EXACTLY the same voltage as measured in step 9 (unity gain).

5.2 Power Supply

REF.	TRIMMER	TRIM PROCEDURE
R5	+5 VOLT SET	1. Monitor the power supply's +15 volt output with a digital voltmeter. 2. Adjust R5 for exactly +15.00 volts.
R11	-15 VOLT SET	1. Set R5 (+15 volts) first. 2. Put the digital voltmeter's ground lead on the power supply's -15 volt output and put the meter's plus lead on the power supply's ground output. 3. Adjust R11 for exactly +15.00 volts (reversed polarity).

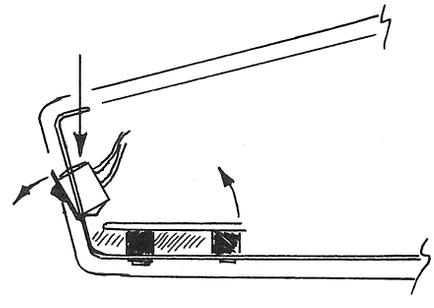
SECTION 6 ASSEMBLY/DISASSEMBLY

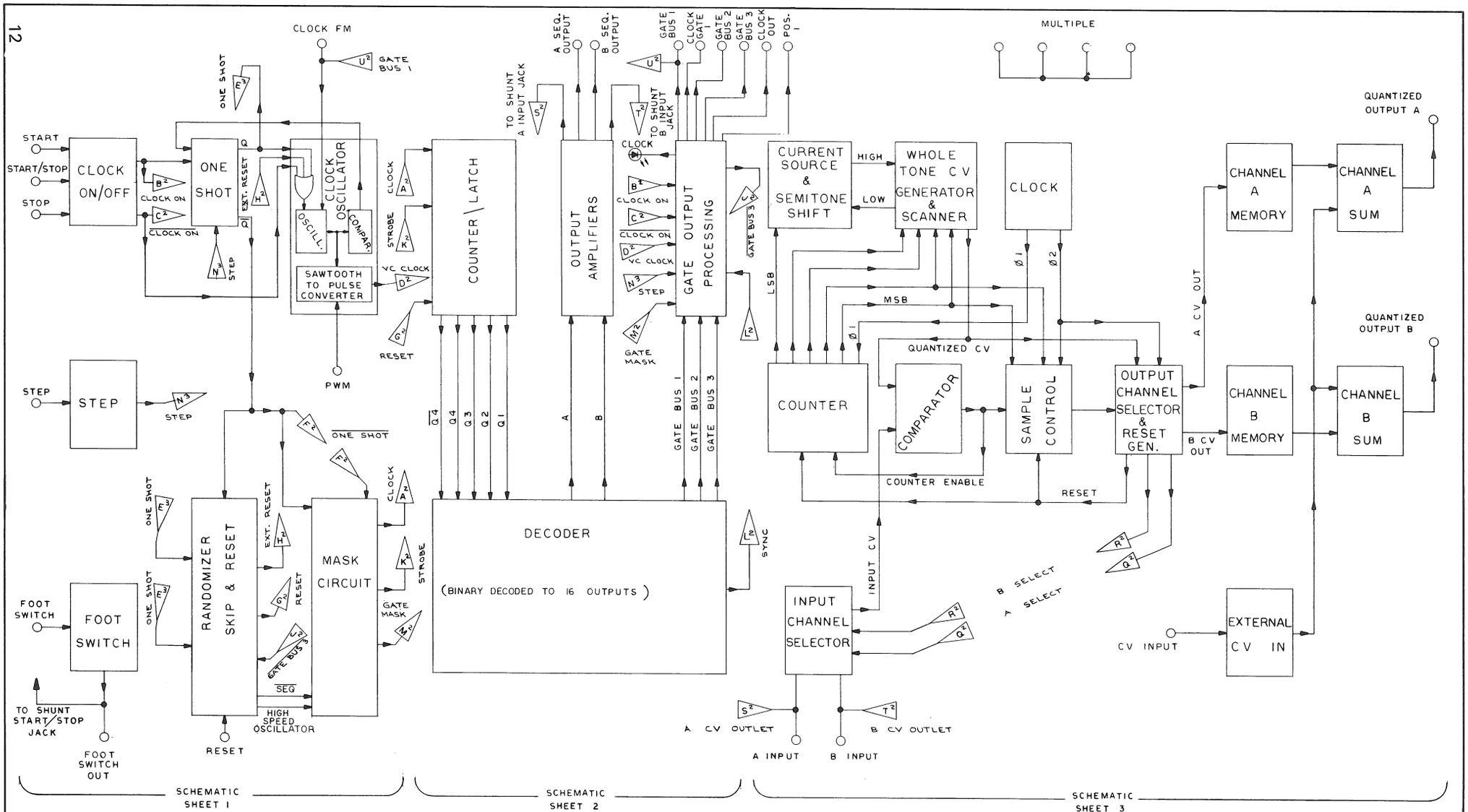


1. To Prevent shock when trouble shooting, unplug the sequencer and mount the power supply on the outside rear panel *(see above illustration).*

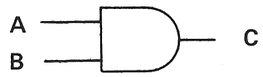
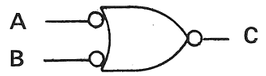
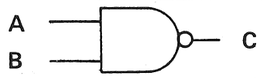
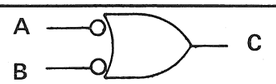
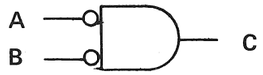
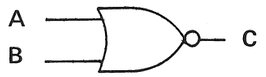
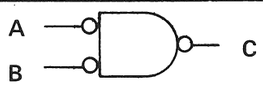
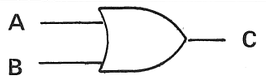
2. To remove the main printed circuit board, remove 11 bolts *(illustrated above),* remove all slider knobs on the front panel, and gently push on the shafts of the sliders until the board pops loose.

3. To remove the lower jack board assembly, remove the jack nuts on the lower front panel. Then pull the bottom of the power switch out so that the jack board clears the power switch *(see illustration to right).*





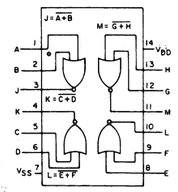
1601 SEQUENCER BLOCK DIAGRAM

AND	OR	A	B	C
		0	0	0
		0	1	0
		1	0	0
		1	1	1
		0	0	1
		0	1	1
		1	0	1
		1	1	0
		0	0	1
		0	1	0
		1	0	0
		1	1	0
		0	0	0
		0	1	1
		1	0	1
		1	1	1

CMOS INTEGRATED CIRCUITS

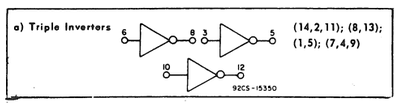
CD4001AE

QUAD 2 INPUT NOR

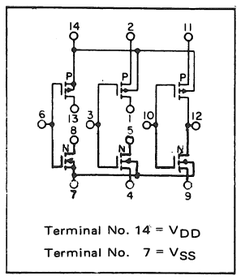


CD4001A

CD4007AE

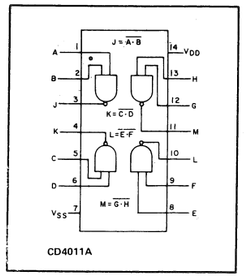


DUAL COMPLEMENTARY PAIR PLUS INVERTER



CD4011AE

QUAD 2 INPUT NAND



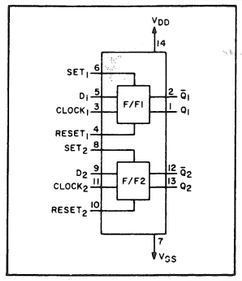
CD4011A

CD4013AE

TRUTH TABLE

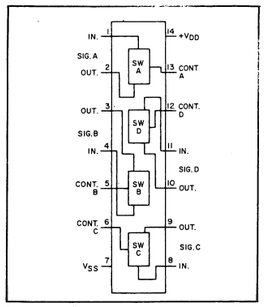
CL	D	R	S	Q	$\bar{Q}$	
↑	0	0	0	0	1	NO CHANGE
↑	1	0	0	1	0	
↓	X	0	0	Q	$\bar{Q}$	
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

DUAL 'D' TYPE FLIP-FLOP



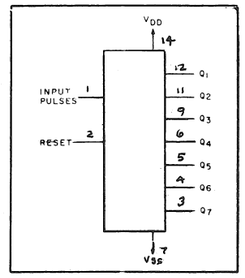
CD4016AE

QUAD BILATERAL SWITCH



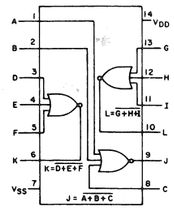
CD4024AE

7 STAGE BINARY COUNTER



CD4025AE

TRIPLE 3 INPUT NOR



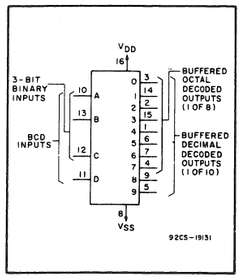
CD4025A

CD4028AE

BINARY TO OCTAL DECODER

TABLE I – TRUTH TABLE

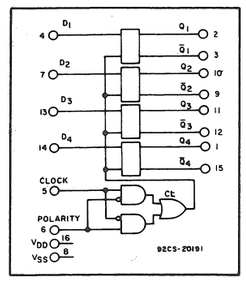
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1



CD4042AE

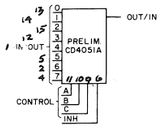
QUAD CLOCKED 'D' LATCH

CLOCK	POLARITY	Q
0	0	D
↑	0	LATCH
1	1	D
↓	1	LATCH



CD4051AE

8 CHANNEL MULTIPLEXER (SIGNAL GATE)

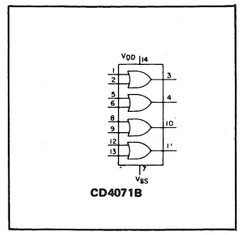


INPUT STATES				"ON" CHAN
INHIBIT	C	B	A	CD4051A
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	*	*	*	NONE

* = Don't care condition

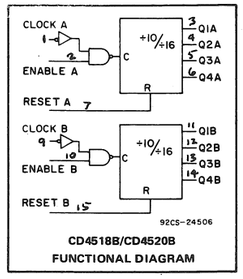
CD4071BE

QUAD 2 INPUT OR



CD4520BE

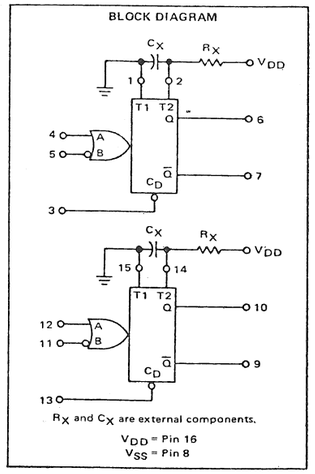
DUAL BINARY UP COUNTER

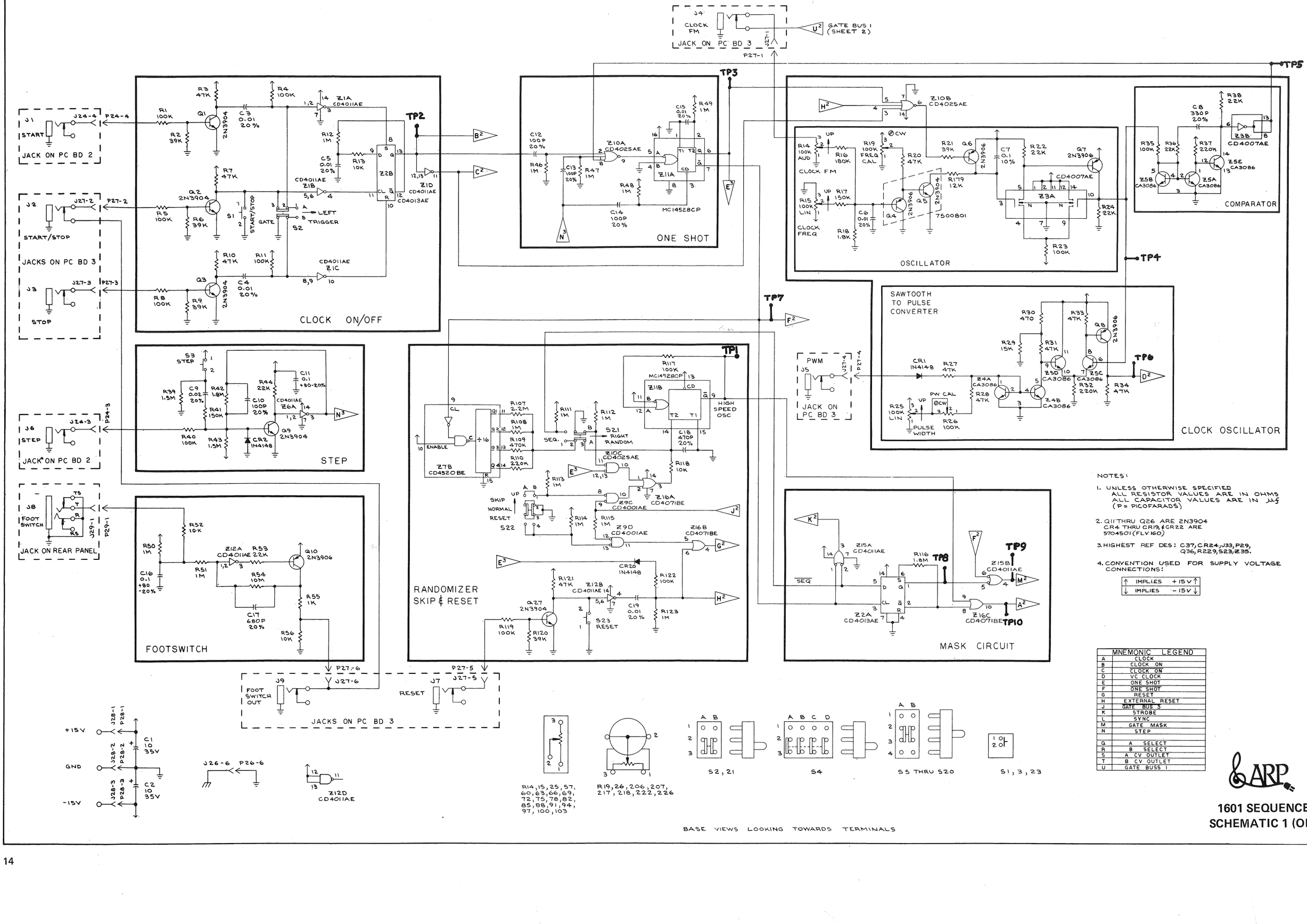


CD4518B/CD4520B
FUNCTIONAL DIAGRAM

MC14528CP

DUAL MONOSTABLE MULTIVIBRATOR





NOTES:

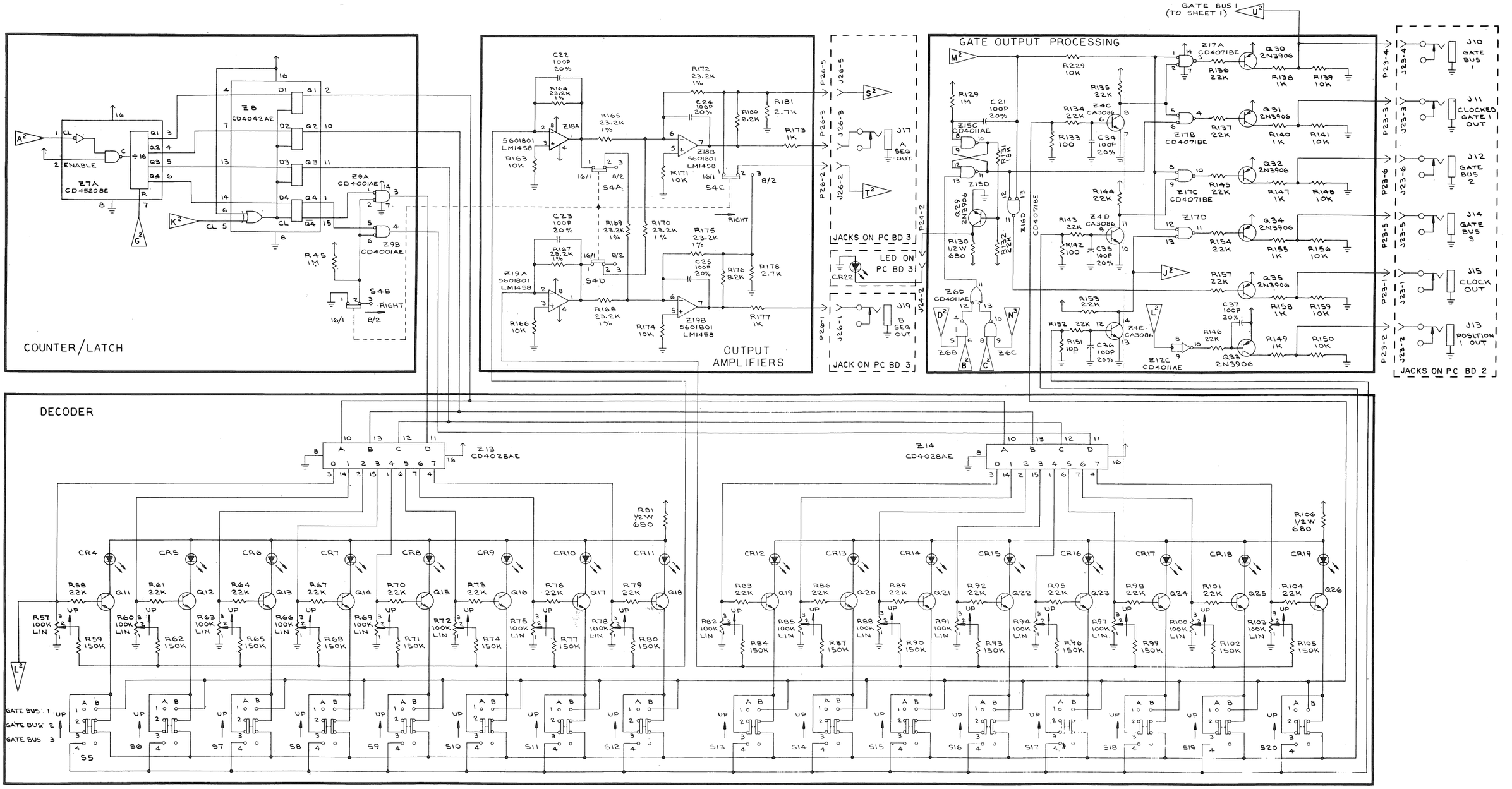
1. UNLESS OTHERWISE SPECIFIED ALL RESISTOR VALUES ARE IN OHMS ALL CAPACITOR VALUES ARE IN μf (P = PICOFARADS)
2. Q1 THRU Q26 ARE 2N3904 CR4 THRU CR19, & CR22 ARE 5704501 (FLV 160)
3. HIGHEST REF DES: C37, CR24, J33, P29, Q36, R229, S23, Z35.
4. CONVENTION USED FOR SUPPLY VOLTAGE CONNECTIONS:

↑	IMPLIES + 15V ↑
↓	IMPLIES - 15V ↓

MNEMONIC	LEGEND
A	CLOCK
B	CLOCK ON
C	CLOCK ON
D	VC CLOCK
E	ONE SHOT
F	ONE SHOT
G	RESET
H	EXTERNAL RESET
J	GATE BUS 3
K	STROBE
L	SYNC
M	GATE MASK
N	STEP
Q	A SELECT
R	B SELECT
S	A CV OUTLET
T	B CV OUTLET
U	GATE BUSS 1

BASE VIEWS LOOKING TOWARDS TERMINALS

1601 SEQUENCER SCHEMATIC 1 (OF 3)



	MNEMONIC LEGEND
A	CLOCK
B	CLOCK ON
C	CLOCK ON
D	VC CLOCK
E	ONE SHOT
F	ONE SHOT
G	RESET
H	EXTERNAL RESET
J	GATE BUS 3
K	STROBE
L	SYNCE
M	GATE MASK
N	STEP
Q	A SELECT
R	B SELECT
S	A CV OUTLET
T	B CV OUTLET
U	GATE BUS 1

ARP

1601 SEQUENCER
SCHEMATIC 2 (OF 3)

CURRENT SOURCE AND SEMITONE SHIFT

R191 324K 1%
R192 332K 1%
R193 332K 1%
R194 392K 1%
R195 1K 1%
R196 39.2K
R197 10K 1%
R198 1K 1%
C29 0.01 20%
Q36 2N3906
Z29A 5601801 LM1458

WHOLE TONE CV GENERATOR AND SCANNER

Z20 5704101
Z21 CD4051AE
Z22 CD4051AE
Z27D CD4001AE
Z29B 5601801 LM1458

CLOCK

TP1 TP2
Ø2 Ø1
Z31C CD4007AE
Z31B Z31A
R190 470K
R189 820K
C28 100P 5%

CHANNEL A MEMORY

A OFFSET ADJUST
R206 100K LIN
R204 100K
R208 100K
C32 0.01 20%
Z34A 5601801 LM1458
R202 10K
C30 0.005 20%
R210 10K
Z32 CD4007AE

CHANNEL A SUM

R217 1K LIN A MOD ADJUST
R219 9.76K 1%
R227 10K 1%
R212 10K 1%
R226 1K LIN
R225 10K 1%
Z34B 5601801 LM1458
R228 1K
QUANTIZED OUTPUT A
J 21
P24-5 J24-5
JACK ON PC BD 2

TP13
TP17
TP18
TP19
TP20
TP21
RESET

COUNTER

Z25 CD4024AE
Z24D CD4011AE

COMPARATOR

R186 10K
Z23 5601901 LM301AN
R188 10K
C27 3.3P 10%
R187 10K
CR23 IN4148

SAMPLE CONTROL

Z24A CD4011AE
Z24B CD4011AE
Z28B CD4013AE

OUTPUT CHANNEL SELECTOR AND RESET GENERATOR

Z28A CD4013AE
R201 1K
CD4016AE
R199 1M
CR24 IN4148
Z27A CD4001AE
Z30C
Z24C CD4011AE
Z27B CD4001AE
R200 1M
Z27C CD4001AE

CHANNEL B MEMORY

B OFFSET ADJUST
R207 100K LIN
R205 100K
R209 100K
C33 0.01 20%
Z35A 5601801 LM1458
R203 10K
C31 0.005 20%
R211 100K
Z33 CD4007AE

CHANNEL B SUM

R218 1K LIN B MOD ADJUST
R220 9.76K 1%
R223 10K 1%
R213 10K 1%
R222 1K LIN
R221 10K 1%
Z35B 5601801 LM1458
R224 1K
QUANTIZED OUTPUT B
J22
P24-1 J24-1
JACK ON PC BD 2

JACKS ON PC BD 3
A INPUT
J16
J25-3 P25-3
B INPUT
J18
J25-2 P25-2

INPUT CHANNEL SELECTOR

Z30A CD4016AE
Z30B CD4016AE
R182 10K
R183 10K
R184 3.9M
R185 10K
Z26B 5601801 LM1458
C26 .001 20%

MULTIPLE
J30
J31
J32
J33
JACKS ON PC BD 3

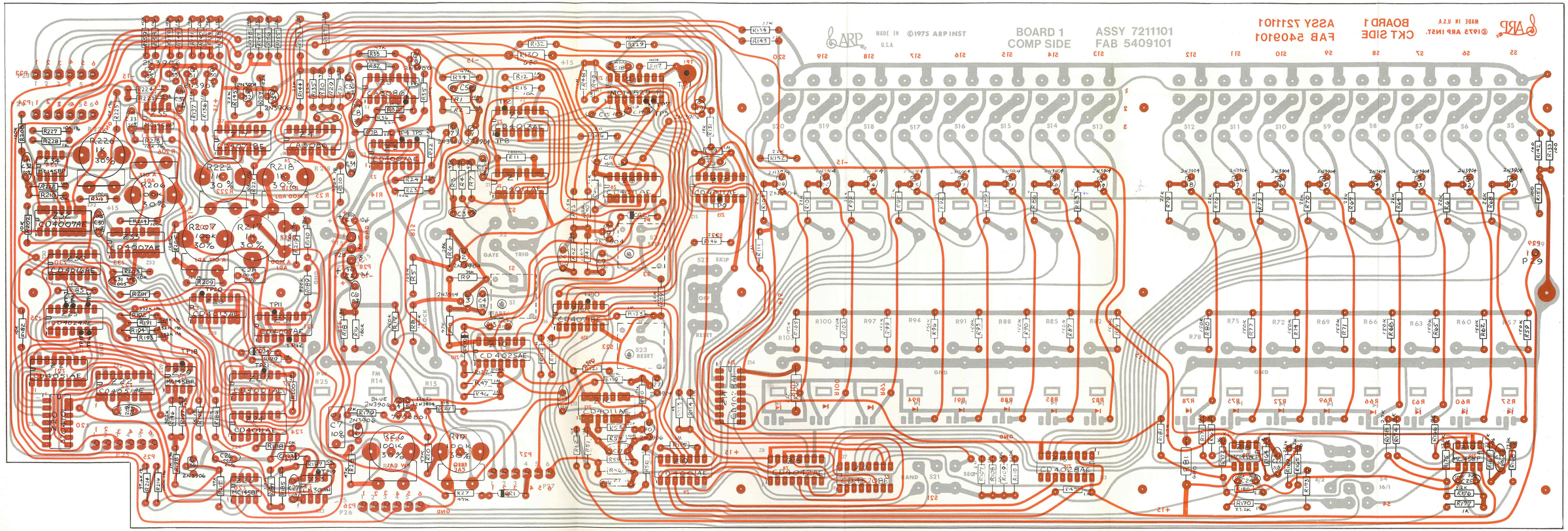
CV INPUT
J20
J24-6 P24-6
JACK ON PC BD 2

EXTERNAL CV IN

R216 100K 1%
R214 97.6K 1%
R215 47K
Z26A 5601801 LM1458

ARP

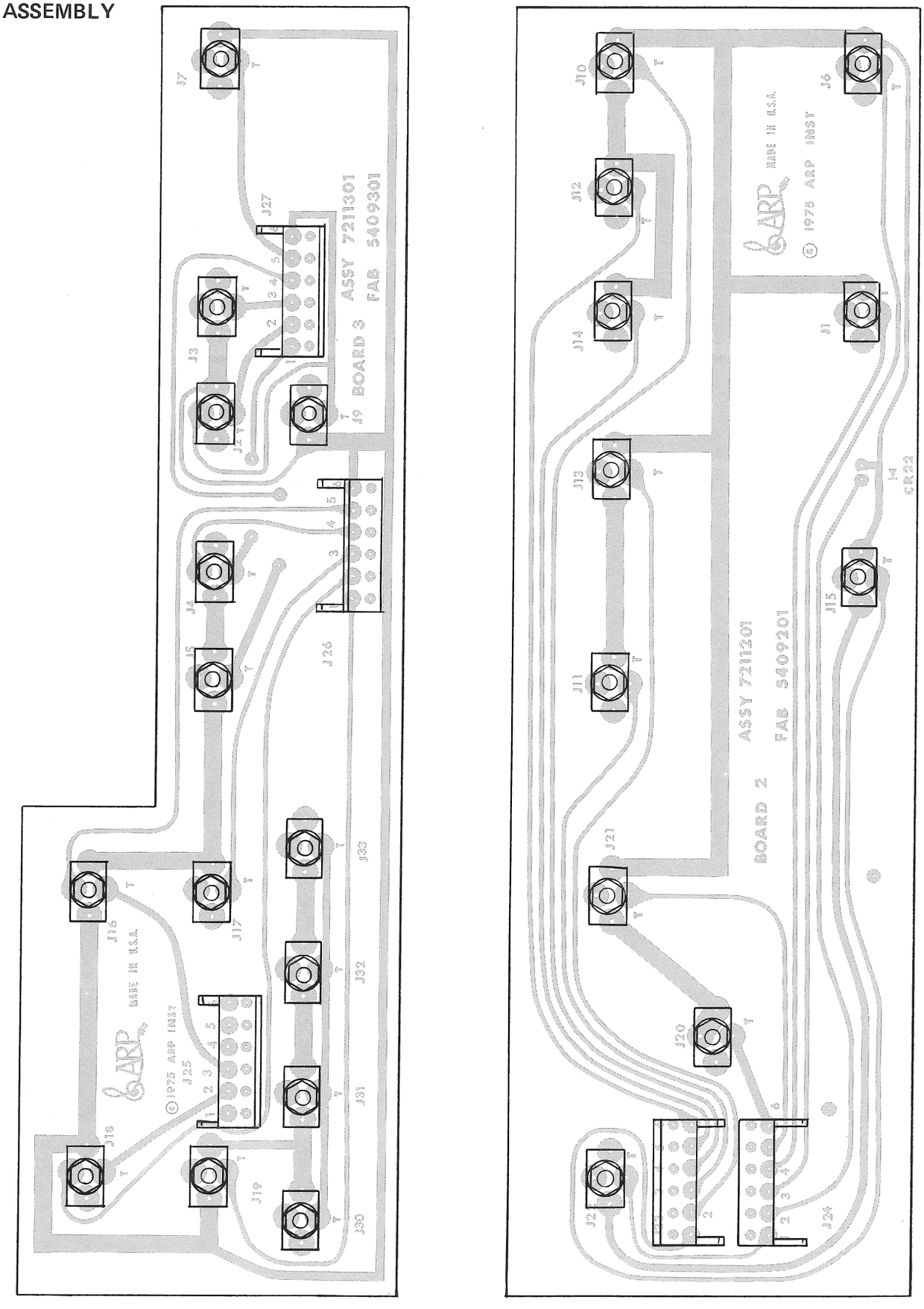
1601 SEQUENCER
QUANTIZER SECTION
SCHEMATIC 3 (OF 3)



COMPONENT SIDE

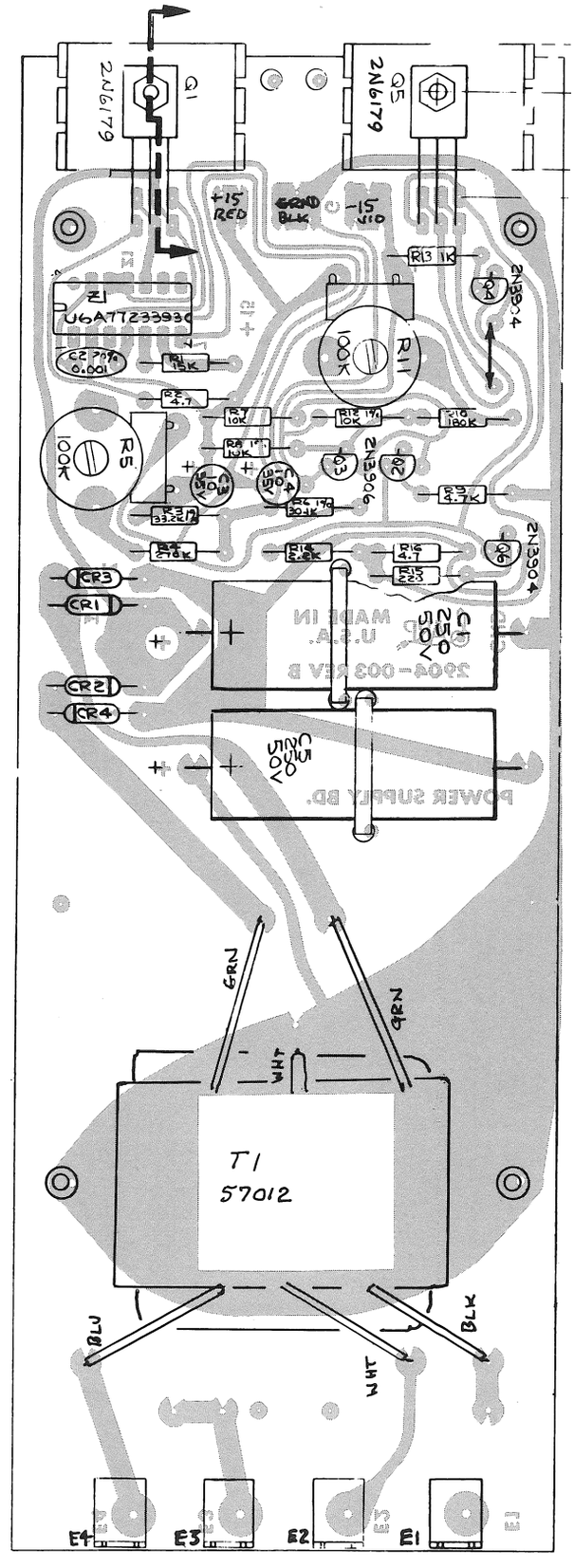
1601 SEQUENCER
MAIN P.C. BOARD
ASSEMBLY

1601 SEQUENCER JACK BOARDS ASSEMBLY

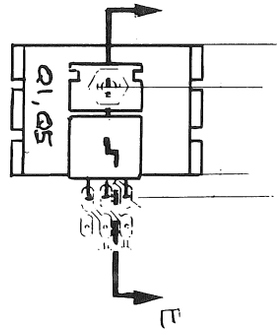


POWER SUPPLY LAYOUT
BOARD NO. 2904-003

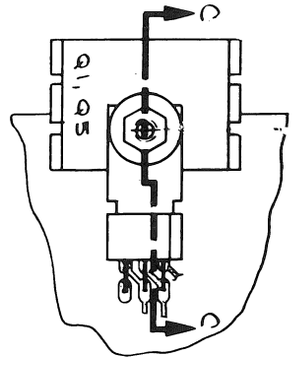
BOARD LAYOUT
COMPONENT SIDE VIEW

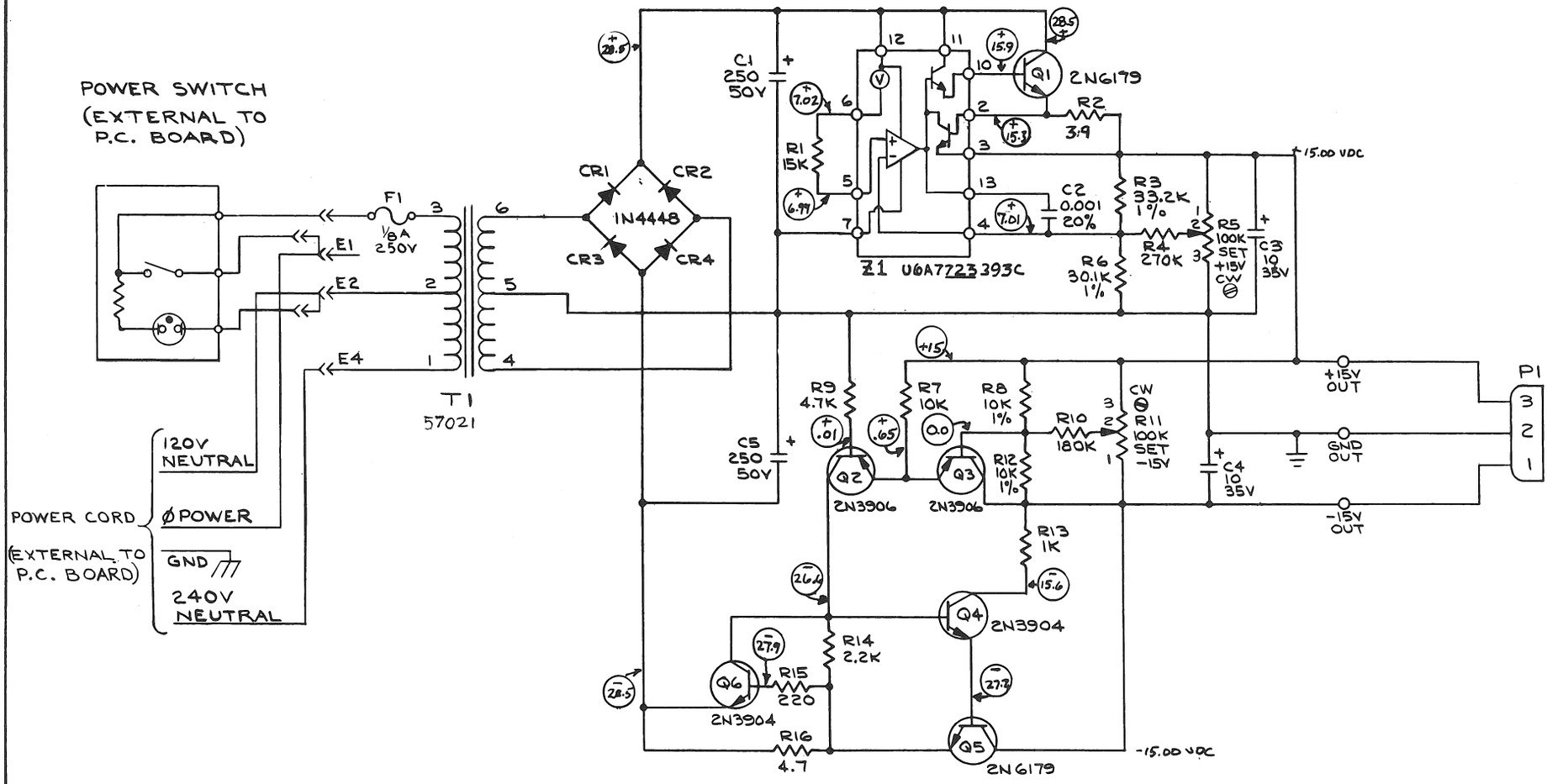


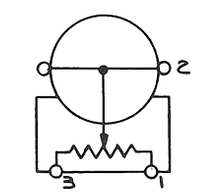
MOUNTING ALTERNATE
TRANSISTORS 2N5298 & 2N5494



MOUNTING ALTERNATE
TRANSISTOR D40D4/2N6179







R5, 11
BASE VIEW
(LOOKING TOWARD
TERMINALS)

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTER VALUES ARE IN OHMS
   CAPACITOR VALUES ARE IN μf (P=PICOFARADS)
2. HIGHEST REF. DES: Q6, Z1, CR4, C5, R16, , E4, T1 & F1
3. (+0.0) INDICATES TYPICAL VOLTAGES AS READ WITH A DVM.

ARP.

POWER SUPPLY SCHEMATIC
BOARD NO. 2904-003

PARTS LIST

BOARD 1

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
CR1,2,20,23,24	1200301	IN4148	DIODE, SIGNAL
CR4-19	5704801		DIODE, LIGHT EMITTING
Q4,5	7500801		TSTR ASSY, NPN/PNP
Q1,2,3,9,11-27	1302901	2N3904	TSTR, NPN, GP
Q6,7,8,10,29-36	1303001	2N3906	TSTR, PNP, GP
Z4,5	1400501	CA3086	IC, TSTR ARRAY
Z18,19,26,29,34,35	5601801		IC, OP AMPL, DUAL
Z23	5601901		IC, OP AMPL, SELECTED
Z9,27	1404301	CD4001AE	IC, GATE, 4X2I NOR
Z3,31,32,33	1404201	CD4007AE	IC, C MOS PAIR, PLUS INVERTER
Z1,6,12,15,24	1400601	CD4011AE	IC, GATE 4XI NAND
Z2,28	1404401	CD4013AE	IC, DUAL D, FF, SET/RESET
Z30	1404501	CD4016AE	IC, QUAD BILATERAL SWITCH
Z25	1400901	CD4024AE	IC, BINARY COUNTER, 7 BIT
Z10	1404601	CD4025AE	IC, GATE, 3X3I NOR
Z13,14	1404701	CD4028AE	IC, BCD-TO-DECIMAL DECODER
Z8	1404801	CD4042AE	IC, QUAD CLOCKED 'D' LATCH
Z21,22	1404901	CD4051AE	IC, SINGLE 8-CHANNEL MLTPLX
Z16,17	1405101	CD4071BE	IC, GATE, 4X2I OR
Z7	1405201	CD4520BE	IC, DUAL BINARY UP COUNTER
Z11	1405301	MC14528CP	IC, DUAL MONOSTABLE MULTIVIB
Z20	5704101		IC, RESISTOR PACK
R222,226	1000904	U201R102B	POT, ROTARY, 1K, ¼W, 30%
R217,218	1000906	U201R252B	POT, ROTARY, 2.5K, ¼W, 30%
R19,26,206,207	1000915	U201R104B	POT, ROTARY, 100K, ¼W, 30%
R15,25,57,60,63,66 69,72,75,78,82,85, 88,91,94,97,100, 103	5700703		POT, SLIDE, LIN, 100K, 1/3W, 30%
R14	5700702		POT, SLIDE, AUD, 100K, 1/3W, 30%
C1,2	1100612	G-0-010-G-20-0	CAP, TANT, 10UF, 35V, 20%
S1,3,23	1903001	DC-51-01	SWITCH, MOMENTARY, SP
S2,21	1902401	01-481-0006	SWITCH, SLIDE, DPDT
S4	1900701	01-481-0005	SWITCH, SLIDE, 4PDT
S5-20,22	1900601	01-481-0004	SWITCH, SLIDE, DPTT
P23-27	2102901	09-64-1067	CONN, PLUG, WAFER, 6-PIN
	2102801	10-18-2031	CONN, RECEPTACLE, 3-PIN

BOARD 2

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
CR22	5704501		DIODE
J1,6,10-15,20-22	2101201	142A	JACK TINI-D
	2503301	MP52	CLIP, MOUNTING, LED

BOARD 3

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
J2,3,4,5,7,9,16, 17,18,19,30,31, 32,22	2101201	142A	JACK TINI-D
J25,26,27	2101803	09-52-3062	CONN, BODY, PLUG, 6-PIN

POWER SUPPLY

REFERENCE	ARP PART NUMBER	ARP/MFG NUMBER	DESCRIPTION
CR1-4	1200401	IN4448	RECTIFIER,SILICON,75V,200MA
Q1,5	1303401	2N6179	TSTR, NPN, PWR
Q4,6	1302901	2N3904	TSTR, SILICON, NPN
Q2,3	1303001	2N3906	TSTR, SILICON, PNP
Z1	1401301	U6A7723393C	IC, VOLTAGE REGULATOR
R5,11	1000915	U201R104B	POT, ROTARY, LIN, ¼W, 10%, 100K
C3,4	1100612	G-0-010-G-20-0	CAP TANT, 35V, +50%-20%, 10UF
C1,5	1101701	B41010-250/50	CAP ELECT, 50V, +50%-10%, 250UF
T1	5701101	C2804-008	TRANSFORMER, POWER
F1	1700402	MDV-1/8	FUSE, PIGTAIL, 1/8A, 250V