E-mu Systems, Inc.

applied magic for the arts

EMULATOR II

SCHEMATICS

© 1985 E-mu Systems Inc. Enhanced by The Emulator Archive 2000 www.emulatorarchive.com

EMULATOR II SCHEMATICS

CPU BOARD

Scanner CPU	7-6
Main CPU	7 - 10
Disk Interface	7 - 15
Serial Interfaces	7 - 16
Microcontroller	7 - 17
RAM Timing	7 - 23
RAM Address Control	7 - 24
RAM Buffering	7 - 25
Dynamic RAM	7 - 26
Clocks and Reset	7 - 30
Power and Connectors	7 - 31
Piggyback Memory	7 - 32

OUTPUT BOARD

Power Supply

Sample/Hold	7 - 39
Timers	7 - 40
Filter Select	7 - 41
Input Analog	7 - 42
SAR	7 - 43
Channels 0 - 7	7 - 44
Mixer	7 - 52
Connectors and Power	7 - 53
Keyboard	7 - 54

(C) 1985, E-mu Systems, Inc., Santa Cruz, Ca. All rights reserved.









































































































