

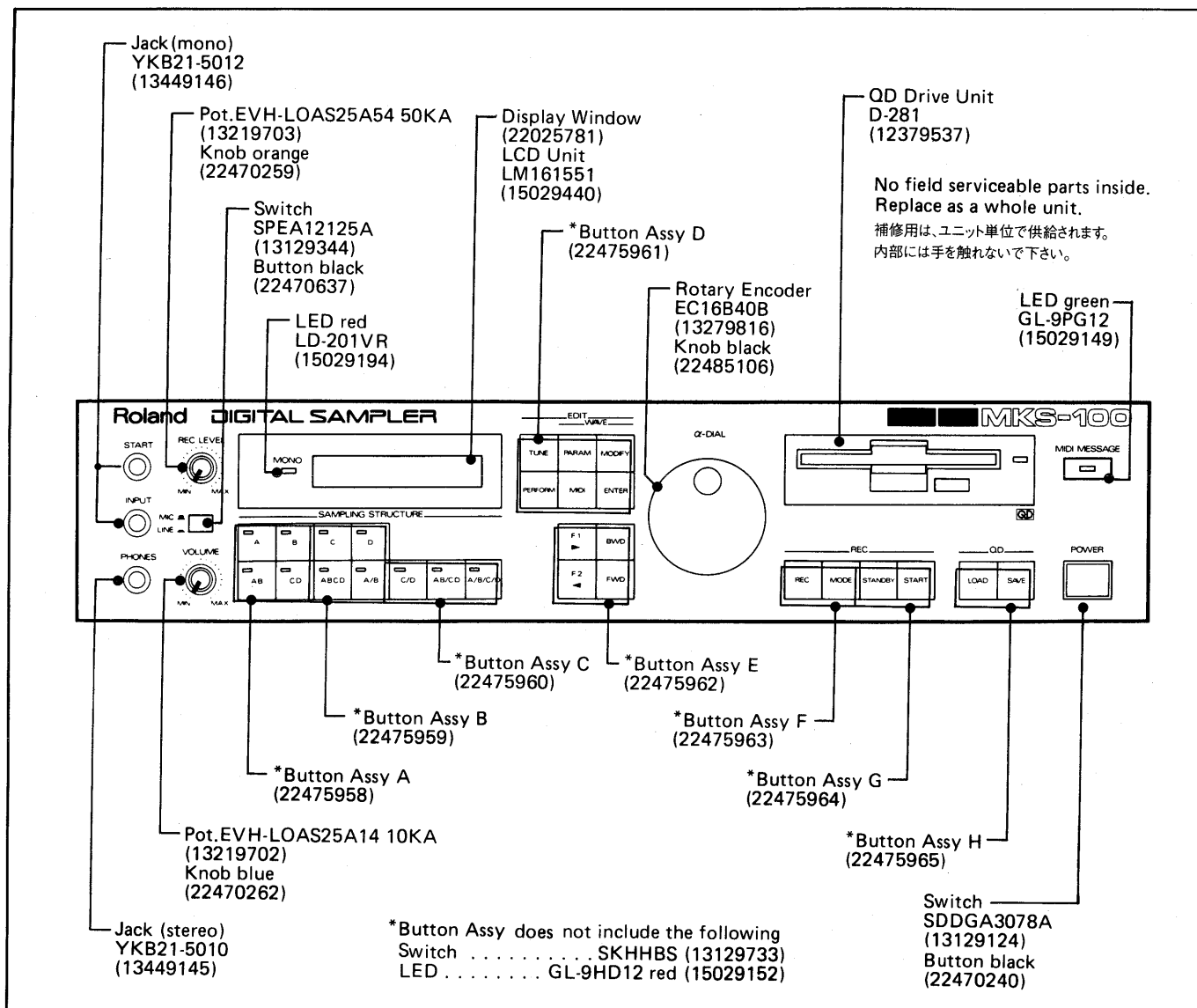
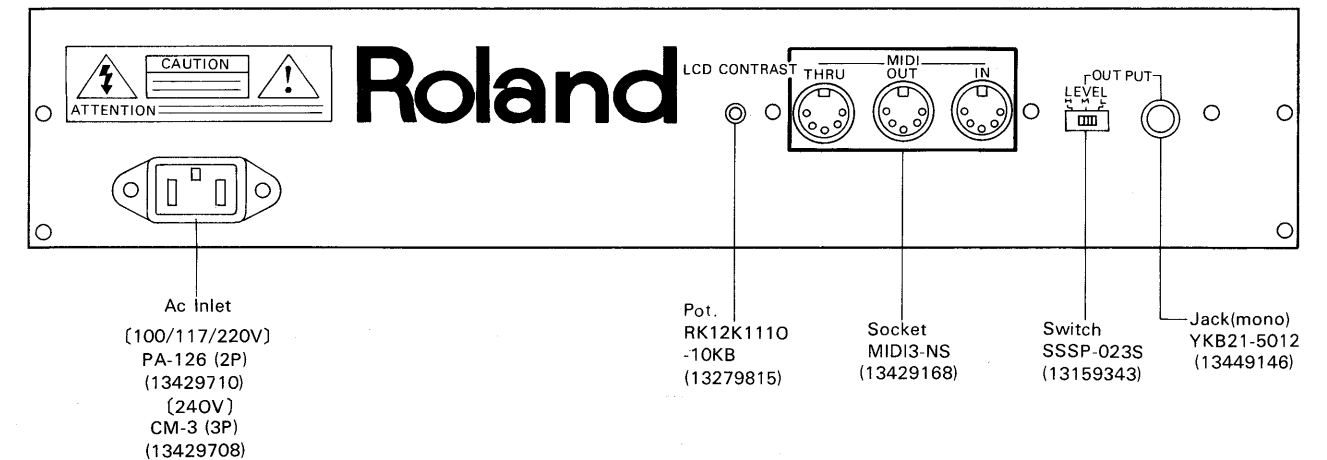
MKS-100

SERVICE NOTES

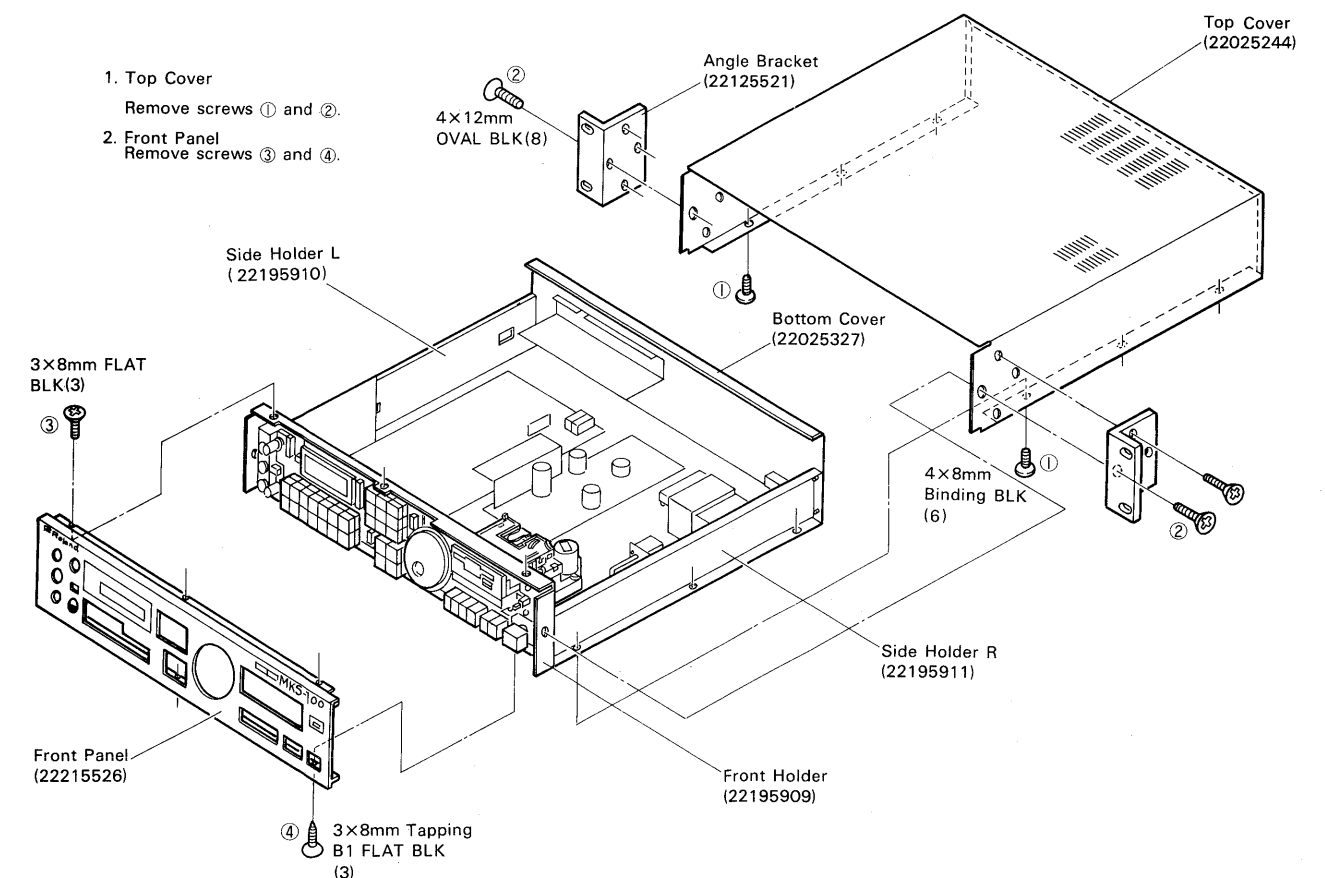
First Edition

SPECIFICATIONS

QUICK DISK	: Front Loading Type	DELAY	Delay Time	: 0 - 1.7 sec
	1 Drive		AUTO BEND	
	Capacity 32k words/side		ABEND Depth	: 0 - -32 semitone
SAMPLING SYSTEM		ARPEGGIO	ARP Rate	: 0.8Hz - 20Hz
	Sampling Rate		EXT-GATE-PLAY	
	: 30kHz/15kHz		TRG Gate Time	: 0 - 12.7 sec
	Data Format		INPUT MIC	: -50dBm
	: 12 bits, Linear		LINE	: -20dBm
	D/A Converter		OUTPUT H	: 0dB
	: 16 bits		M	: -15dB
	Sampling Time		L	: -30dB
	: 4 sec (A → B → C → D)		Power Consumption	: 19W
	1 sec (A, B, C, D)		Dimensions	: 483(W) x 410(D) x 90(H) mm
	@30kHz sampling rate			19-1/4 x 16-1/8 x 3-7/16 in.
	8 sec (A → B → C → D)		Weight	: 7 kg/15 lb. 7 oz.
	2 sec (A, B, C, D)			
	@15kHz sampling rate			
Wave Memory	: 128k words			
	4 Tone banks (32k words) A, B, C, D			
Key Mode	: Whole/one split/three split			
LFO	Rate			
	: 0.085Hz - 12Hz			
	Delay			
	: 0 - 4.4 sec			
TUNE	Master Tune			
	: ±100 cents			
	Detune			
	: ±50 cents			
	Bank Tune			
	: ±50 cents			
	Loop Tune			
	: ±50 cents			



DISASSEMBLING PROCEDURE



PARTS LIST

CASING

22215526	Front Panel	フロント・パネル
22025244	Top Cover	トップ・カバー
22025327	Bottom Cover (Chassis)	ボトム・カバー
22025781	LCD Cover (Display Window)	ディスプレイ・カバー
22195909	Front Holder	フロント・ホルダー
22195910	Side Holder Left	サイド・ホルダー 左
22195911	Side Holder Right	サイド・ホルダー 右
22195912	Jack Holder	ジャック・ホルダー
22195913	Output Holder	アウトプット・ホルダー
22195914	Power Switch Holder	電源スイッチ・ホルダー
22195915	QD Holder	QDホルダー
22125521	Angle Bracket	ラック・アングル
22355334	Base (Rubber Foot)	ゴム足

KNOB, BUTTON

22485106	Knob blk φ45	α-DIAL
22470259	Knob org	REC LEVEL
22470262	Knob blu	VOLUME
22470240	Button blk	POWER
22470637	Button blk	MIC/LINE
22475958	Button Assy A blk	A, B, AB, CD
22475959	Button Assy B blk	C, D, ABCD, A/B
22475960	Button Assy C blk	C/D, AB/CD, A/B/C/D
22475961	Button Assy D blk	TUNE, PARAM, MODIFY PERFORM, MIDI, ENTER
22475962	Button Assy E blk	F1 →, F2 ←, BWD, FWD
22475963	Button Assy F blk	REC, MODE
22475964	Button Assy G blk	STANDBY, START
22475965	Button Assy H blk	LOAD, SAVE
Button Assemblies do not include Switch and LED. ボタン・ユニットはスイッチおよびLEDを含みません。		

AC CORD (DETACHABLE)

13439825	DC-320-J01	100V
13439812F0	UC-704-J01	117V
13439813F0	EC-210-J06	220V
23495110	5722 660 4606	240V England
13439814F0	SC-415-J06	240V Australian

JACK, SOCKET

13449145	YKB21-5010 (stereo)	PHONES
13449146	YKB21-5012 (mono)	OUTPUT, INPUT, START
13429168	MIDI3-NS triplet socket	MIDI IN/OUT/THRU
13429525	IS28B08CT 28P IC socket	EPROM (Main Board)
13429710	PA-126 2P AC inlet	100/117/220V
13429708	CM-3 3P AC inlet	240V

SWITCH

13129124	SDDGA3078A	POWER
13129733	SKHHBS light touch	keypad
13159343	SSSP-023S (shorting)	OUTPUT LEVEL
13129344	SPEA12125A (non-shorting)	MIC/LINE

FUSE

(100/117V)			
12559343	GG5 630mA	(F1) pri.	
12559335	GG5 1A	(F2,F3) sec.	
12559400	UL-TSC-2A-N1	(F4) sec.	
(220/240V)			
12559541	S504 200mA (or 12559507 CEE-200mA)	(F1) pri.	
12559542	S504 250mA (or 12559508 CEE-250mA)	(F2,F3) sec.	
12559550	S506 1.6A (or 12559521 CEE-1.6A)	(F4) sec.	

FUSE CLIP

12199550	H0446	Power Supply Board
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TRANSFORMER

22455463U0	245-463U0	Power	100/117/220/240V
12449552	D32-45	EL inverter	

PLATE

22125195	212-195	Plate	Power Transformer (common to S-10, αjuno and MC-500)
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DISK DRIVE UNIT

12379537	D-281	2.8 inch quick disk drive unit No field serviceable parts inside. Replace by unit. 交換はユニット単位で行って下さい。 個別部品の補修用は用意されていません。
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LCD UNIT

15029440	LM161551	with EL, PCB, and wirings No order accepted for attaching parts. Replace by a unit. 補修用は、ユニットで供給されます。 (基板、EL、ワイリングを含む)
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INDUCTOR

12449265	ELE-H102KA	1mH	
12449229	FK0B-160MH15		Line filter
13529105	OSS310-550223S		EMI filter
22445280	244-280 TFB-3	fc=6KHz	LC filter
22445281	244-281 TFB-3	fc=12.5KHz	LC filter
22445282	244-282 TFB-3	fc=13.5KHz	LC filter

CRYSTAL

12389760	HC-49/U 26.880MHz	
12389756	HC-49/U 6.5MHz	
12389754	CST 12.0MT2	

IC

<Main Board>		
15179237F0	SAB8032A	CPU
15179798	MBM27C512-25	EPROM
15179334	TC5564PL-20	SRAM
15179362H0	HM50464P-12	64k × 4 DRAM
15179360	MB87013	QD drive interface adapter
15179361	MB89251A	USART
15229834	MB62H195	I/O gate array
15229840	RF5C36	sampler custom IC
15219171	EHK-M06209	D/A converter
15159701	M54522	LED driver
15189111P0	IR9311	comparator
15189194	BA6993	comparator
15159124T0	TC4093BP	quad 2-input NAND schmitt-trigger
15159503	TC40H000P	quad 2-input NAND gate
15159505	TC40H004P	hex inverters
15159510	TC40H074P	dual D-type flip-flops
15169325X0	SN74LS273N	latch
15169514	74HC04P	hex inverters
15169534	74F02	quad 2-input NOR gates
15169546	74F00	quad 2-input NAND gates
15189193	M5238P	J-FET OP amp
15189186	μPC4570C	OP amp (low noise)
15219174	NJU 201AD	analog switch

<Input Board>		
15219157	M5241L	VCA
15189171	M5218P	OP amp
15189186	μPC4570C	OP amp (low noise)

<Output Board>		
15169514	74HC04P	hex inverters
15229706S0	PC910 (or 15229706 TLP552)	optoisolator

<Switch Board 1>		
15169318	74LS138	3 to 8 line decoder/demultiplexer

<Power Supply Board>		
15199117	M5230L	voltage regulator
15199143	SI-3052V	voltage regulator

TRANSISTOR

15119129	2SA1115-E	
15119821	2SB1185-E	
15129107	2SC945-Q	
15129140	2SC2603-E	
15129136	2SC2878A	
15129836	2SD1762-E	

RESISTOR ARRAY

13919320	RMLS 6-333J	33k × 6
13919303	RMLS 8-333J	33k × 8

DIODE

15019125	1SS133 (or 1519103 1S2473)		
15019208	1SR35-200A	200V 1A rectifier	
15019245	1B4B41	100V 1A bridge rectifier	
15019272	2B4B41-LC2	100V 2A bridge rectifier	
150196120Z	05Z-5.1Z	zener	

(LED)

15029149	GL-9PG12	green,package white	MIDI MESSAGE
15029152	GL-9HD12	red,package white	SAMPLING STRUCTURE
15029194	LD-201VR	red	MONO MODE

PCB ASSEMBLY

79366160	Main Board	(PCB 22925330)	
	Can be substituted by S-10 Main Board with minor modification. See Main Board PCB layout section of this manual for details. S-10のメイン基板で代用可能。メイン基板の頁の説明参照。		
79366211	Power Supply Board 100/117V	(PCB 22925332 1/2)	
79366214	Power Supply Board 220/240V	(PCB 22925332 1/2)	
	Two versions are the same except for fuses. A different version with correct fuses may be supplied if line voltage is specified in the order sheet. Also compatible with S-10 P.S. BD with minor modification. See P.S. board layout section for details.		
	電源基板はヒューズを除けば共通使用が可能です。 代用基板が供給された場合はヒューズ値に注意して下さい。 また、S-10の電源基板とも一部を除けば共通。基板図の頁参照。		
79366110	Encoder Board	(PCB 22925332 2/2)	
79366060	Switch Board 1	(PCB 22925405)	
79366120	Input Board	(PCB 22925406 1/4)	
79366180	Output Board	(PCB 22925406 2/4)	
79366080	Switch Board 2	(PCB 22925406 3/4)	
79366100	LED Board	(PCB 22925406 4/4)	

POTENTIOMETER

13219702	EVH-L0AS25A14	10KA	VOLUME
13219703	EVH-L0AS25A54	50KA	REC LEVEL
13279815	RK12K1110-10KB		LCD CONTRAST
(Trimmer)			
13299191	EVN-D3AA00B23	2KB	Power Supply Board VR1
13299577	EVM-39GA00B22	200B	Power Supply Board VR2

ROTARY ENCODER

13279816	EC16B40B	40 pulses/rotation incremental	α-DIAL
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WIRING ASSEMBLY

23495517	CC-M62-10P	L=280mm	QD Wiring
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CAPACITOR

13659213M0	ECET25R472SW	4700μF 25V	electro
13659222M0	ECET35R222SW	2200μF 35V	electro
13619102N0	CS15E1A6R8K1S	6.8μF 10V	tantalum
13589328	ECQ-P1H392JZ3	0.0039μF	polypropylene
13529104	DE7150F472MVA1-KC	0.0047μF	line bypass

CONNECTOR

(straight type)

13439260	5267-03A	3P wafer assy	
13439261	5267-04A	4P wafer assy	
13439262	5267-05A	5P wafer assy	
13439263	5267-06A	6P wafer assy	
13439265	5267-08A	8P wafer assy	
13439269	5267-09A	9P wafer assy	
13439277	5267-14A	14P wafer assy	
13439334	CP-M60-10	10P wafer assy	Main Board CN12

(right angle type)

13439285	5268-03A	3P wafer assy	
13439286	5268-07A	7P wafer assy	

MISCELLANEOUS

12569149S0	CR2032-T12	Lithium Battery	
22465498	246-498	Heat Sink	Power Supply Board
22150401	215-401	Joint (to button)	
22140207	214-207	Connection Rod	
22150402	215-402	Joint (to switch)	
22220319	222-319	Button Frame	POWER switch
22195450	219-450	LED Holder	LED Board
22245460	224-460	LCD Dust Cover	
22245154	224-154	Encoder Mask	α-DIAL
22245155	224-155	Volume Mask	REC LEVEL,VOLUME

COMMERCIALLY AVAILABLE

(Accessories 出荷時附属品)

22375545	S9-S10-001	QD Sound Library (Drum set)
22375546	S9-S10-002	QD Sound Library (Strings/chorus)
22375547	S9-S10-003	QD Sound Library (Combination)
23430675S0	LP-25	Connection Cord (2.5m)
23485167	348-167	MIDI/SYNC Cable (1m)

(Options オプション)

-----	L-101 — 111	QD Sound Libraries
22375551	Roland QD-10	2.8 inch Quick Disk (10pcs)
-----	MSC-25	MIDI/SYNC Cable (2.5m)
-----	MSC-50	MIDI/SYNC Cable (5m)
-----	DP-2	Pedal Switch

互換性について

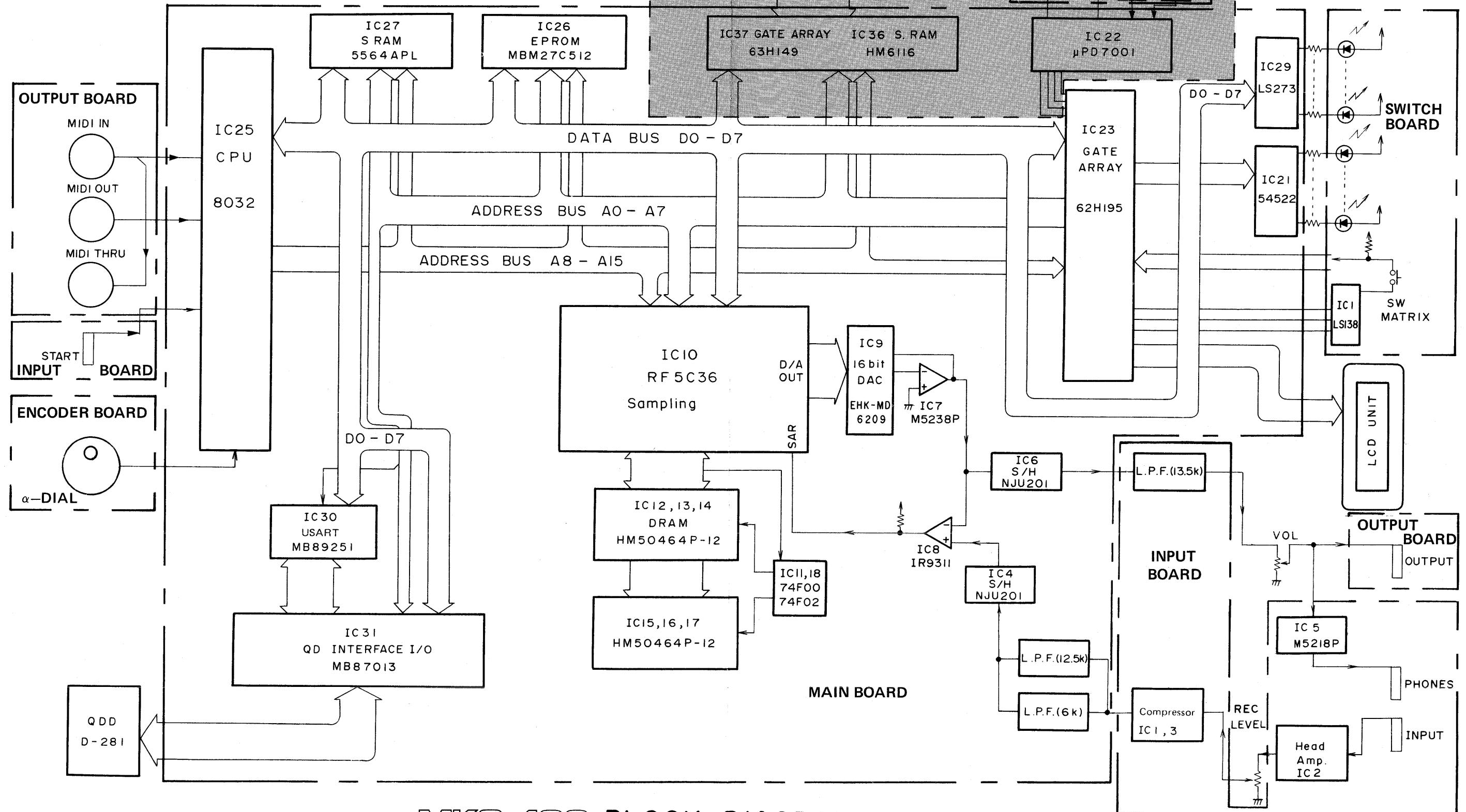
MKS-100のメインボードは、基本的にはサンプリング・キーボード S-10用と同じです。斜線部が主な相違点です。このため、S-10のメイン・ボードをMKS-100に流用することが出来ます。詳細は11頁を参照して下さい。

BLOCK DIAGRAM

COMAPTIBILITY

Main board of MKS-100 is fabricated on the same pcb as for S-10, keyboard sampler, with major difference being as shown by the shaded box.

This information will help should it become necessary to substitute S-10 main board to MKS-100's. See P.11 for details.



MKS-100 BLOCK DIAGRAM

CIRCUIT DESCRIPTIONS

回路解説

1. CPU Main Board IC25 8032

- Major Tasks of the CPU;
- LED lighting, LCD driving, IC27 (working RAM) reading/writing
 - IC10 (Sampling IC) reading/writing
 - MIDI transmitting/receiving
 - Rotary encoder reading

1. CPUメインボード IC25 8032A

- CPUの主たる機能は次の通りです。
- LED点灯、LCD駆動、ワーキングRAM IC27への書き込み/読み出し
 - サンプリングIC IC10 (RF5C36) への書き込み/読み出し
 - MIDIデータ送受信
 - ロータリエンコーダーの読み込み

2. I/O Gate Array Main Board IC23 62H195

Most of addressing for I/O's and memories and some of the functions are done through I/O gate array IC23.

Shown below are the address map to be set by 62H195 and the block diagram of 62H195. (Fig. 1)

2. I/Oゲートアレイ メインボード IC23 62H195

上記のI/Oおよびメモリのアドレスの設定や動作の全部または一部は、I/Oゲートアレイを通じて行なわれます。62H195のブロックダイアグラムおよびアドレスマップを下に示します。(Fig.1)

3. Sampling IC Main Board IC10 RF5C36

The Roland custom IC RF5C36 plays a key role in the sampling system. The process is illustrated mainly with the aid of photos, diagrams and charts.

NOTE (See Fig. 2)

The system clock for the sampling system is based on the Xtal connected across IC10 pins 70 and 71. Left under an unstable condition, X1 will sometimes cause TP7 (RAS) to be kept high. This problem will be found on ealier products. This can be solved by adding 10PF (C32) across main board IC10 pin 71 and the ground point.

3. サンプリング IC10 RF5C36

サンプリングICを中心とした音声データの流れの概略をブロック図、写真、チャート等を主体に説明します。

サンプリングシステムのシステムクロックは、IC10ピン70、71間に接続されているX1に基づいて発生します。このXtal回路が不安定な場合TP7 (RAS) がHになったままとなります。初期製品では発振安定用コンデンサC32 10PFがIC10ピン71とグランド間に入っていないためこのような現象を生じるものがあります。無い場合は取り付けて下さい。(Fig.2)

Fig. 1 (2. I/O Gate Array Main Board IC23 62H195)

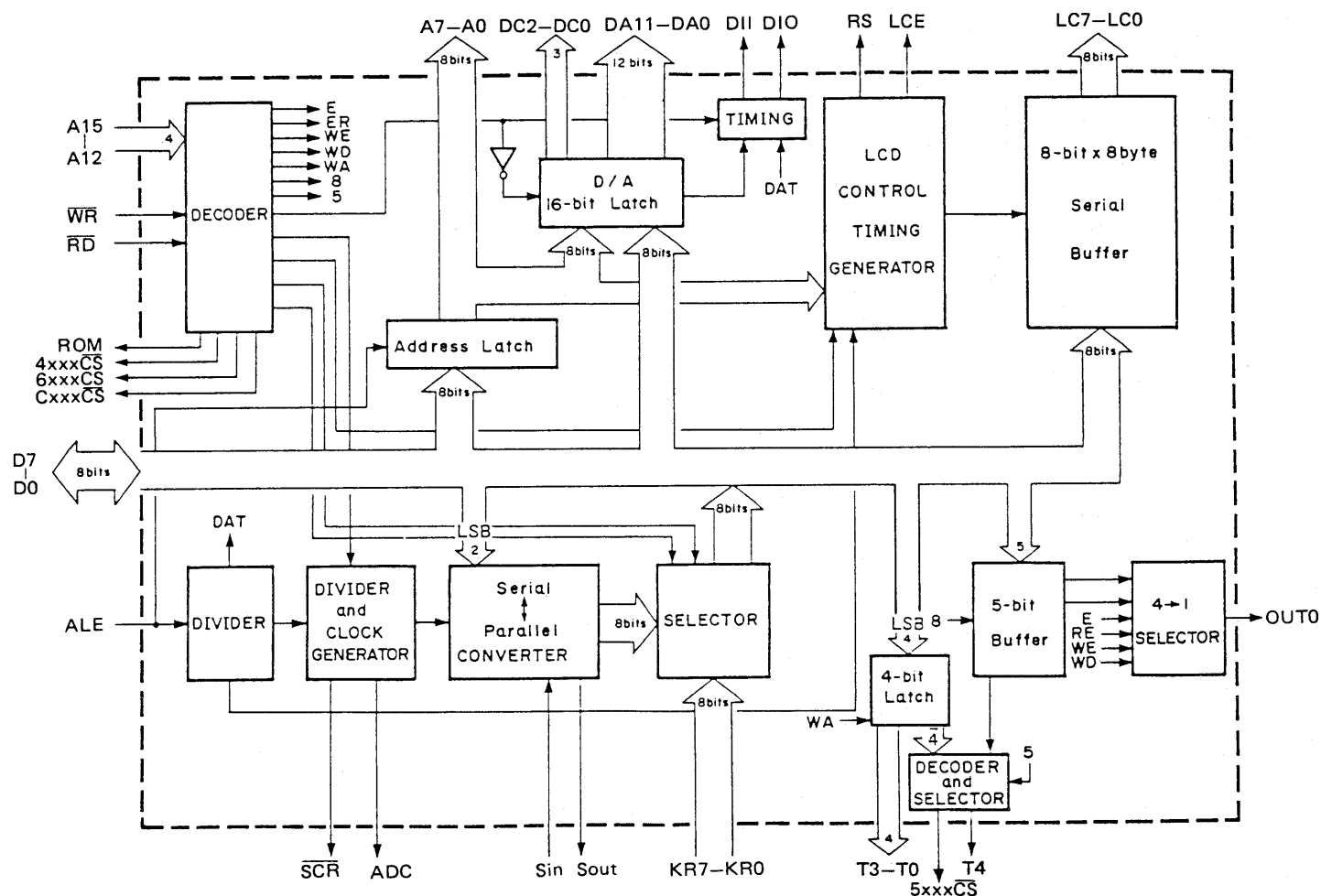


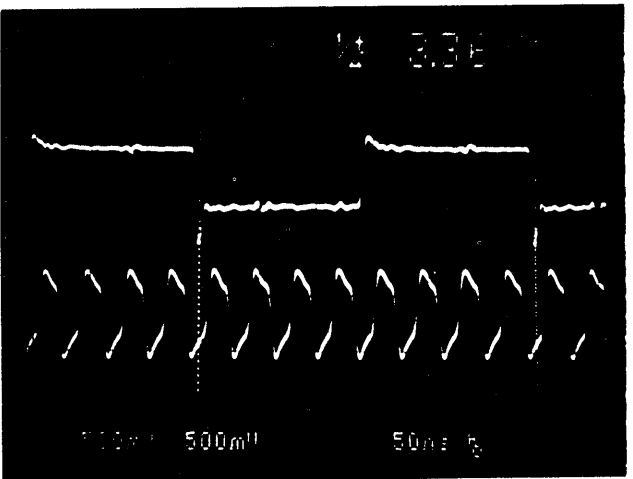
Fig. 2 (3. Sampling IC Main Board IC10 RF5C36)

	PSEN	RD	WR
FFFF			
F000		IC10 RF5C36 CS	IC10 RF5C36 CS
E000			
D000			IC29 LED LATCH PULSE
C000			
B000			
A000		SW SCAN SELECT	SW SCAN DATA
9000			IC21 LED DATA
8000			LCD DATA
7000		IC27 SRAM 5564APL CS	IC27 SRAM 5564APL CS
6000			
5000		IC31 MB87013 CS	IC31 MB87013 CS
4000			
3000			
2000			
1000			
0000			

Main board

TP7
RAS CLK

IC10
Pin 71



3-1. Loading From QD

(See Fig. 3)

3-2. Sampling External Audio Input

IC3b of the output board can accommodate input signals between -50dBm and 0dBm. The compressor consisting of IC3a, 4, 5, Q7, etc. relieves the subsequent digital circuits from overload.

3-1. QDからのデータロード

(Fig.3参照)

3-2. 外部音声入力のサンプリング

アウトプットボードのIC3bの許容入力は -50 ~ 0dBm です。

次段のIC3a、4、5、Q7はコンプレッサであって、過大入力を抑制します。

メインボード上ではサンプリングクロックの設定に応じてL1、またはL2の出力が選ばれます。

Sampling Rate	IC4		OUTPUT
	Pin 8	Pin 9	
30kHz	L	H	L1
15kHz	H	L	L2

Fig. 3 (3-1. Loading From QD)

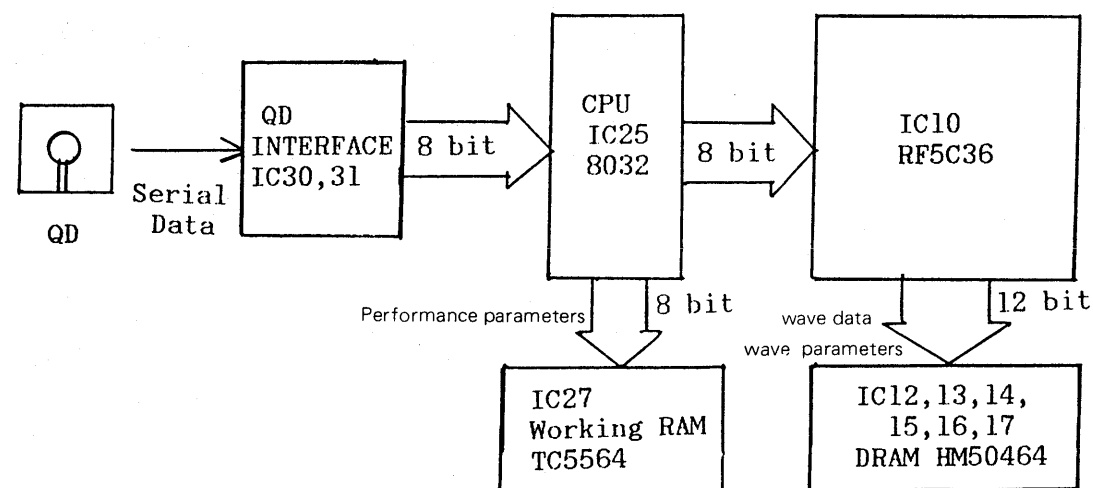


Fig. 4 (3-2. Sampling External Audio Input)

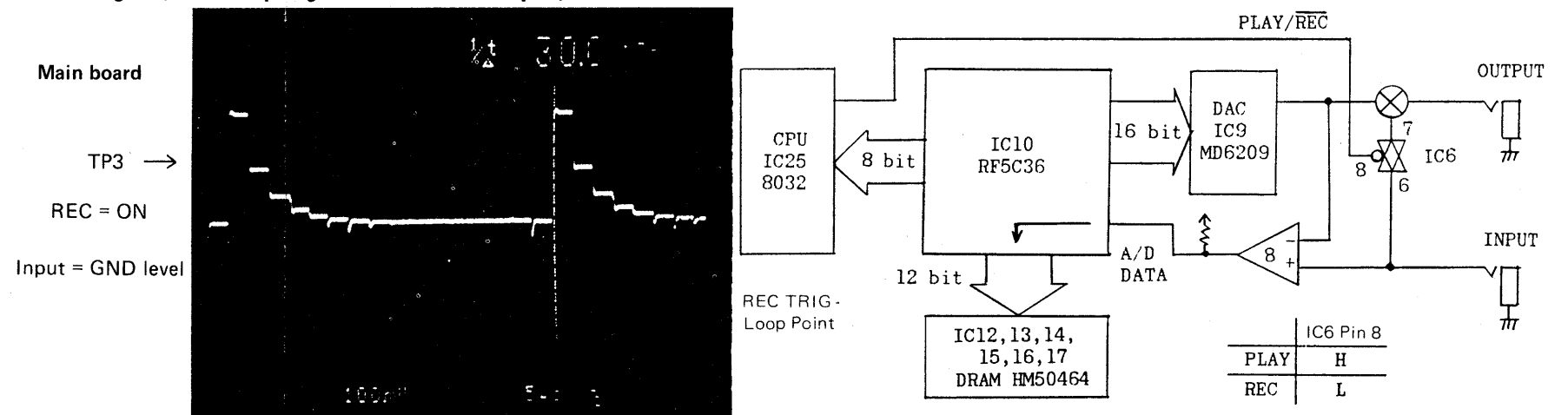
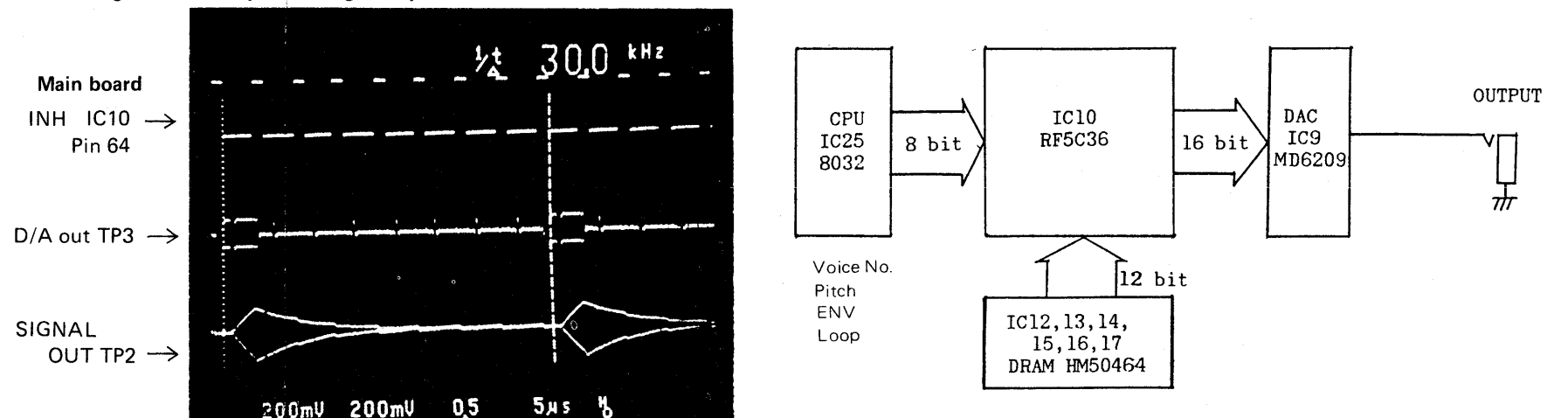


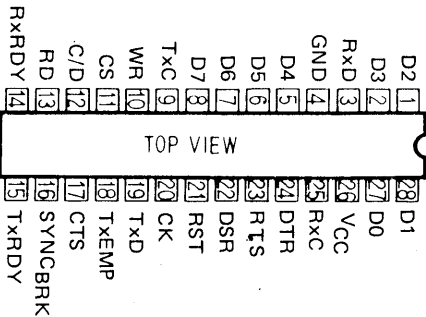
Fig. 5 (3-3. Reproducing Sampled Sound)



QUICK DISK SYSTEM

Data transfer between the CPU and the disk is accomplished through the QD interface consisting of IC USART and IC31 QD drive interface I/O.

USART MB89251A

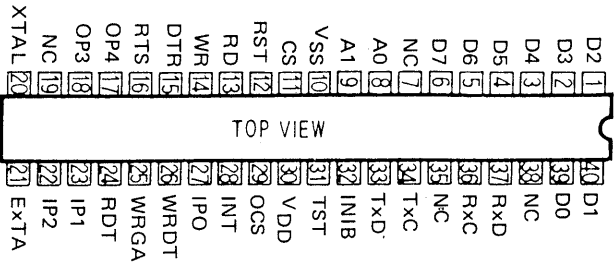


PIN NUMBER	PIN NAME	I/O	DESCRIPTION
3	RxD	I	(Receiver Data) This input is the data read from QD via IC31. QDから読み出されたデータ
25	RxC	I	(Receiver Clock) Controls the rate at which the data from QD is received. QDからの受信データと同期をとるための受信クロック
19	TxD	O	(Transmitter Data) This output is to be transmitted to QD. QDへの送信データ
9	TxC	I	(Trasmitter Clock) Controls the rate at which the data is to be transmitted to QD. QDへの送信データと同期をとるための送信クロック
10	WR	I	(Write) A "low" on this input informs the MB89251A that the CPU is writing data or controls to the MB89251A. CPUからのWRITE信号。LOWで MB89251Aへの書き込み可能
11	CS	I	(Chip Select) A "low" on this input selects the MB89251A. アドレスをデコードした信号。LOWでMB89251Aがセレクトされる
13	RD	I	(Read) A "low" on this input informs the MB89251A that the CPU is reading data or controls from the MB89251A. CPUからのREAD信号。LOWでMB89251A から読み込み可能。
14	RxRDY	O	(Receiver Ready) Not used 未使用
15	TxRDY	O	(Transmitter Ready) Not used 未使用
16	SYNC BRK	I/O	(Sync Break) Not used 未使用
17	CTS	I	(Clear to Send Data) Not used, Pulled low 未使用. LOW
18	TXEMP	O	(Transmitter Empty) Not used 未使用
20	CK	I	(Clock) A clock of 3.25MHz is used to generate internal device timing. 3.25MHz入力。
21	RST	I	(Reset) A "high" on this input forces the MB89251A into idle mode. HIGHでRESET. LOWで通常動作。
22	DSR	I	(Data Set Ready) Used to confirm the position of the read/write head. Should be set to low only when the read/write head is positioning over a read/write sector. QDのヘッド位置を知るための入力。ヘッドが読み書き可能な位置にある時にLOWが入力されること。
23	RTS	O	(Request to Send) Not used 未使用
24	DTR	O	(Data Terminal Ready) A "low" on this ouptput is used when recording is performed on QD. To be inverted at IC31 output, pin 25 WRGA. QDに書き込む時にLOWを出力。DTR信号はIC31(MB87013)内部のインバタを通してピン25のWRGAからQDドライブに加えられる
26	VCC	-	+5V
4	GND	-	

クイックディスクシステム

QDインターフェイスはメインボード上のIC30 USART とIC31 QDドライブ・インターフェイスI/Oから成っています。

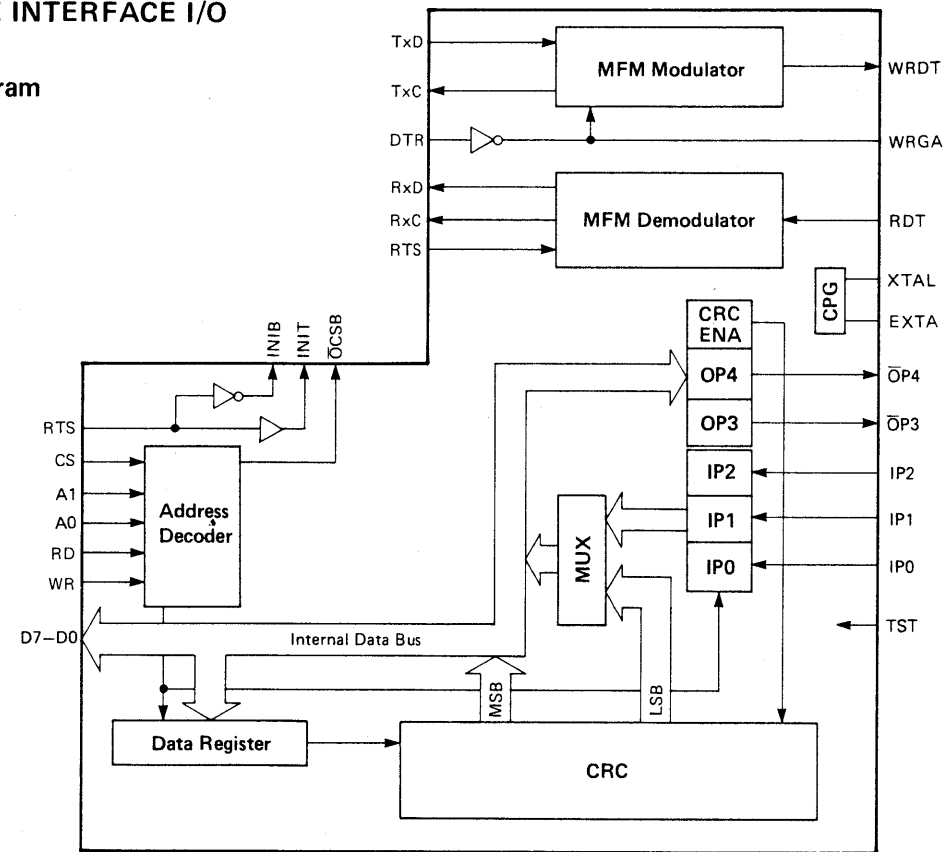
QD DRIVE INTERFACE ADAPTER MB87013



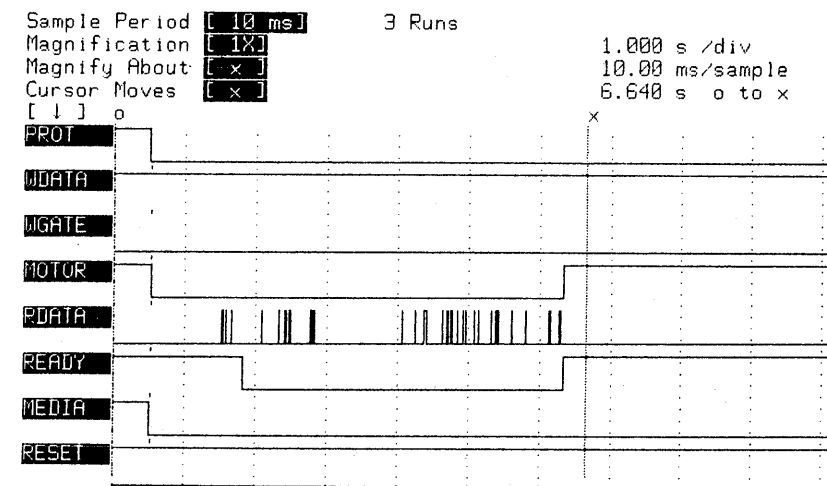
PIN NUMBER	PIN NAME	I/O	DESCRIPTION																																																																						
1-6, 39, 40	D7-D0	I/O	Data Bus: To be connected to the CPU data bus. データバス、CPUのデータバスに接続。																																																																						
12	RST	I	Reset: A low on this input resets the MB87013. リセット入力端子。LOWでMB87013はリセットされる。																																																																						
13	RD	I	Read: Can be used to enable data onto the data bus from MB87013. Active low. MB87013からデータを読み出す為の、アクティブ.ローのリードパルス入力端子。																																																																						
14	WR	I	Write: Used to write data into the MB87013 register. Active low. MB87013へデータを書き込む為の、アクティブ.ローのライトパルス入力端子。																																																																						
11	CS	I	Chip Select: Can be used in conjunction with a low RD, low WR, A0 and A1 to gain access to internal registers. チップ.セレクト入力端子。RD、WR、A0、A1と 組合せ MB87013の内部レジスタへアクセスすると出来る。																																																																						
			<table><tr><th>CS</th><th>A1</th><th>A0</th><th>RD</th><th>WR</th><th>DATA BUS</th><th>OCS</th></tr><tr><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>Hi-imp</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Hi-imp</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Data Register Write (MB89251A, MB87013)</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>Hi-imp</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Hi-imp</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>CRC Register (MSB) Read</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Data Register Write</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Control Register Read CRC Register (LSB) Read</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Control Register Write</td><td>1</td></tr></table>	CS	A1	A0	RD	WR	DATA BUS	OCS	1	-	-	-	-	Hi-imp	1	0	0	0	0	1	Hi-imp	0	0	0	0	1	0	Data Register Write (MB89251A, MB87013)	0	0	0	1	0	1	Hi-imp	0	0	0	1	1	0	Hi-imp	0	0	1	0	0	1	CRC Register (MSB) Read	1	0	1	0	1	0	Data Register Write	1	0	1	1	0	1	Control Register Read CRC Register (LSB) Read	1	0	1	1	1	0	Control Register Write	1
			CS	A1	A0	RD	WR	DATA BUS	OCS																																																																
			1	-	-	-	-	Hi-imp	1																																																																
			0	0	0	0	1	Hi-imp	0																																																																
			0	0	0	1	0	Data Register Write (MB89251A, MB87013)	0																																																																
			0	0	1	0	1	Hi-imp	0																																																																
			0	0	1	1	0	Hi-imp	0																																																																
			0	1	0	0	1	CRC Register (MSB) Read	1																																																																
			0	1	0	1	0	Data Register Write	1																																																																
			0	1	1	0	1	Control Register Read CRC Register (LSB) Read	1																																																																
0	1	1	1	0	Control Register Write	1																																																																			
8, 9	A0, A1	I	Address: Used to select internal register. 内部レジスタを選択するの用いられる。																																																																						
28	INIT	O	Reset output: Inverted RST. Active high. RSTを反転したアクティブHIGHのリセット信号端子。																																																																						
32	INiB	O	Low active reset output: Buffered RST. RSTをバッファリングしたアクティブLOWのリセット信号 出力。																																																																						
29	OCS	O	Chip Select: Used to select serial interface (MB89251A). シリアル.インターフェースMB89251AのCS信号。 (OCS=CS+A1)																																																																						

33	TxD	I	Transmitter Data: To be re-transmitted to QD after modified frequency modulated. 送信データ入力端子。
34	TxC	O	Transmitter Clock: Controls the rate at which data is transmitted to QD drive. 送信同期クロック出力端子。
37	RxD	O	Receiver Data: Demodulated data read from QD. To be re-transmitted to IC30. 受信データ出力端子。
36	RxC	O	Receiver Clock: Controls the rate at which IC30 receives the data from QD via IC31. 受信同期クロック出力端子。
16	RTS	I	Gate: A low on this input enables transfer of data read from QD to IC30, through RxC and RxD. 受信データを、RxCとRxDに出力する時のゲート。LOWで受信データをMB89251などに転送できる。
15	DTR	I	A low on this input causes MFM modulator to be initialized. MFMモジュレータのイニシャライズ信号入力端子。
26	WRDT	O	Data out: Signal from this output is to be recorded on QD. クイックディスクへのデータ出力端子。
24	RDT	I	Data In: Data read from QD is received through this port. クイックディスクからのリードデータ入力端子。
25	WRGA	O	A high from this output enables recording on QD. クイックディスクはWRGAがHIGHの時、ディスクに データ書き込み 出来る。この端子にはDTRの反転値が出力される。
27	IPO	I	Indicates the status of the WRITE PROTECT switch: With a disk inserted a high IPO represents "WRITE PROTECTED" ライトプロテクトSWをセンスするためのポート。QD が入った状態で、HIGHならプロテクトされたQD。
23, 22	IP1, IP2	I	Used to sense QD: Low=QD inserted, High=QD not inserted. QDの挿入、検出用ポート。 L=挿入、 H=未挿入
18	OP3	O	Used to turn on/off disk unit motor: Low=ON. モータのON・OFFビット。LOWでON
17	OP4	O	This output is connected to RTS. Low OP4 enables MB89251A to recieve data from QD. RTSをコントロール。LOWで受信可能。
20	XTAL		6.5MHz crystal input for internal oscillator. 水晶振動子の接続端子。6.5MHzの水晶接続。
21	EXAL		Not used 未使用
30	VDD		Main power supply: +5V +5V
10	VSS		Circuit GND potential GND
31	TST		Used for test purpose only: must be pulled up to VDD. テスト用端子です。通常VDDにプルアップ。

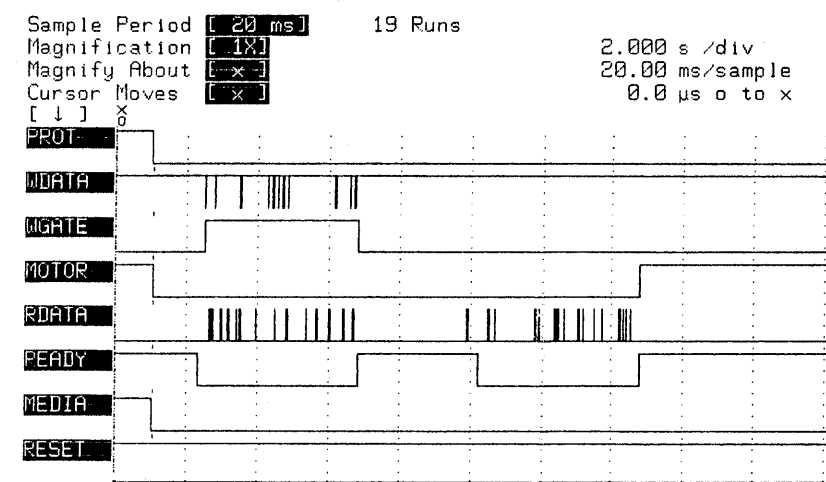
QD DRIVE INTERFACE I/O MB87013 Block Diagram



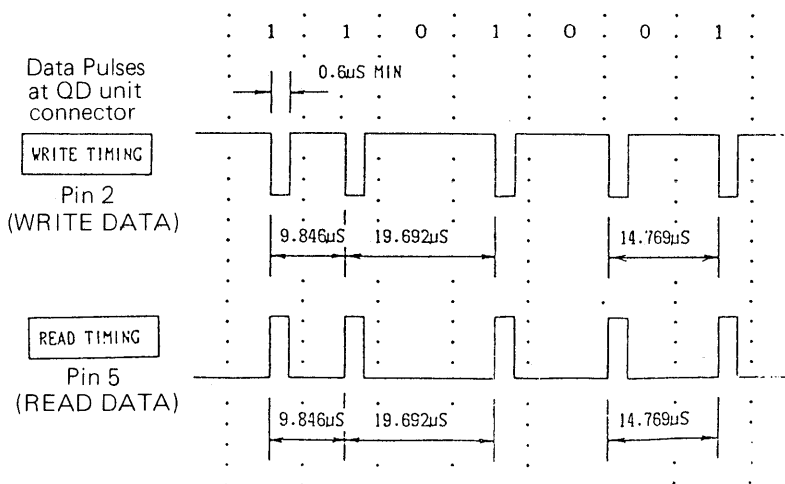
READ TIMING DIAGRAM IN LOAD MODE



WRITE TIMING DIAGRAM IN SAVE MODE



DATA PULSE TIMING



These three diagrams represent waveforms on the drive unit connector (or Main Board CN12).

Note that the data pulses shown in the figure right are of ideal ones and cannot be observed as they drawn.

これら3枚のタイミングチャートは、ドライブユニットのコネクタ (又はメインボードCN12) 上の波形です。

注
右図のデータパルスは理想波形であって、実際にはこの様なきれいなパルス波形とならない。

QD DRIVE UNIT PIN DESCRIPTION TABLE

PIN NUMBER	SIGNAL NAME	I/O	DESCRIPTION
1	WRITE PROTECT	OUT	Indicates whether the recording on the inserted disk is inhibited or not. HIGH : inhibited LOW : not inhibited With a write protected disk inserted, the internal recording circuits are disabled. この信号は、挿入されたディスクが記録許可か禁止かを示します。 "HIGH" : 記録禁止 "LOW" : 記録許可 ライトプロテクトされたディスクが挿入された時ドライブ内部ではライト動作を禁止します。(記録禁止はA, B両面に可能)
2	WRITE DATA	IN	External data input to be recorded. Recorded with high WRITE GATE, a high to low transition of a data reverses the current direction in the read/write head, which records a 1 bit data. この信号は、外部回路より供給される信号で、ディスク上に記録するデータです。 "HIGH" から "LOW" レベルに変わることによりリードライトヘッドに流れる電流を反転させデータビットを記録します。 この記録は、WRITE GATE 信号が "HIGH" レベルの時行えます。
3	WRITE GATE	IN	High WRITE GATE enables recording. この信号が、"HIGH" レベルの時ディスク上にデータを記録出来ます。"LOW" レベルの時は記録できない。
4	MOTOR ON	IN	Low MOTOR ON starts the motor. With High MOTOR ON, an internal MOTOR STOP can stop the motor. ドライブモーターの ON/OFF 制御信号です。この信号を "LOW" にするとモーターが回転します。この信号を "HIGH" にした後、ドライブ内の MOTOR STOP 信号が入るとモーターは停止します。
5	READ DATA	OUT	Pulse-shaped analog signal read from the disk. Contains the unseparated clock and data pulses. このデータは、ディスクから読み出されたアナログ信号をパルスに波形整形したもので、クロックとデータを含んでいます。
6	READY	OUT	Indicates that recording or reading may take place. この信号は、ディスクから読み出し許可、または記録許可を示します。
7	MEDIA SW	OUT	Low state indicates that disk slot lid is closed with a disk inserted. High state represents open lid or closed lid without a disk. ディスクがセットされた状態で蓋をしめていれば "LOW" レベル、蓋が開いているか又はディスクを装着しないか蓋をしめた場合 "HIGH" レベルとなります。
8	RESET	IN	Low for the predetermined period after POWER ON RESET, causing internal READY pulled low and resetting the internal flip-flop for the motor to defeat MOTOR ON. POWER ON RESET 時、一定時間 "LOW" レベルとなる信号で、この信号により (ドライブ内部の) READY 信号を "LOW" にすると共に MOTOR が起動しないように (ドライブ内部の) MOTOR ON/F/F をリセットする。
9	VB		+ 5 V
10	GND		

Diagnostic Program

The diagnostic program incorporated in the MKS-100 checks the following electronic functions as well as the ROM Version number—without demanding disassembling.

NOTE

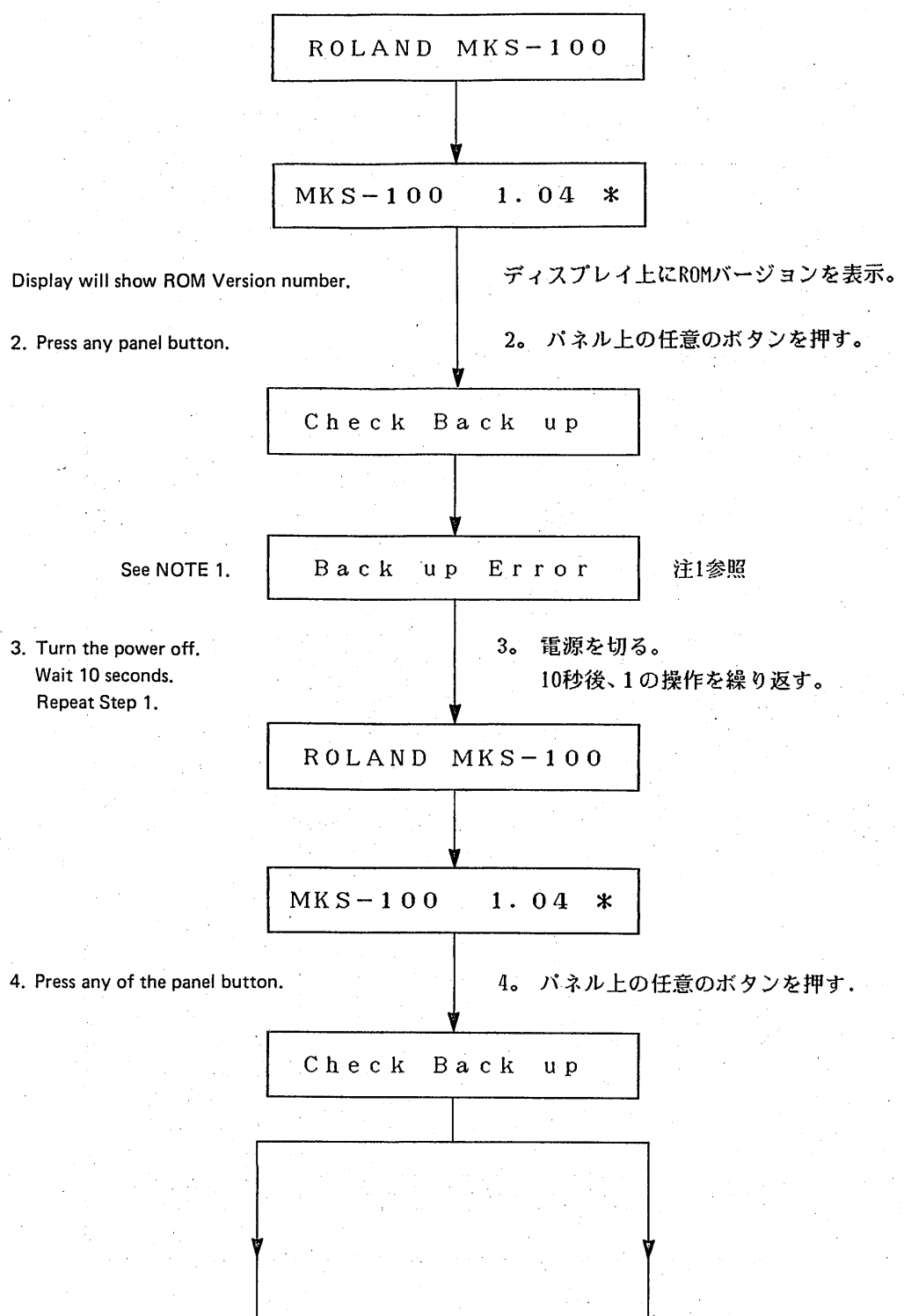
The diagnostic program stops whenever it detects a malfunction and won't go to the next test unless "IGNORE" command is applied externally. IGNORE command can be entered from the panel by pressing PERFORM and MIDI simultaneously.

The program proceeds in the order:

1. ROM (IC26 main board) version number identification
2. Memory backup (lithium battery)
3. S-RAM (IC27 main board)
4. D-RAMs (ICs 12-17 main board)
5. IC10 (factory test use only)
6. Switches and LEDs
7. Rotary encoder
8. QD drive
9. Output
10. MIDI

Entering Test Mode

1. While pressing PERFORM and MIDI turn the power on.



診断プログラム

MKS-100には診断プログラムが内蔵されているので、ROM IC26 のバージョンナンバーのみならず主要回路機能を、パネルを開けることなく点検することが出来ます。診断プログラムは次の順に進みます。

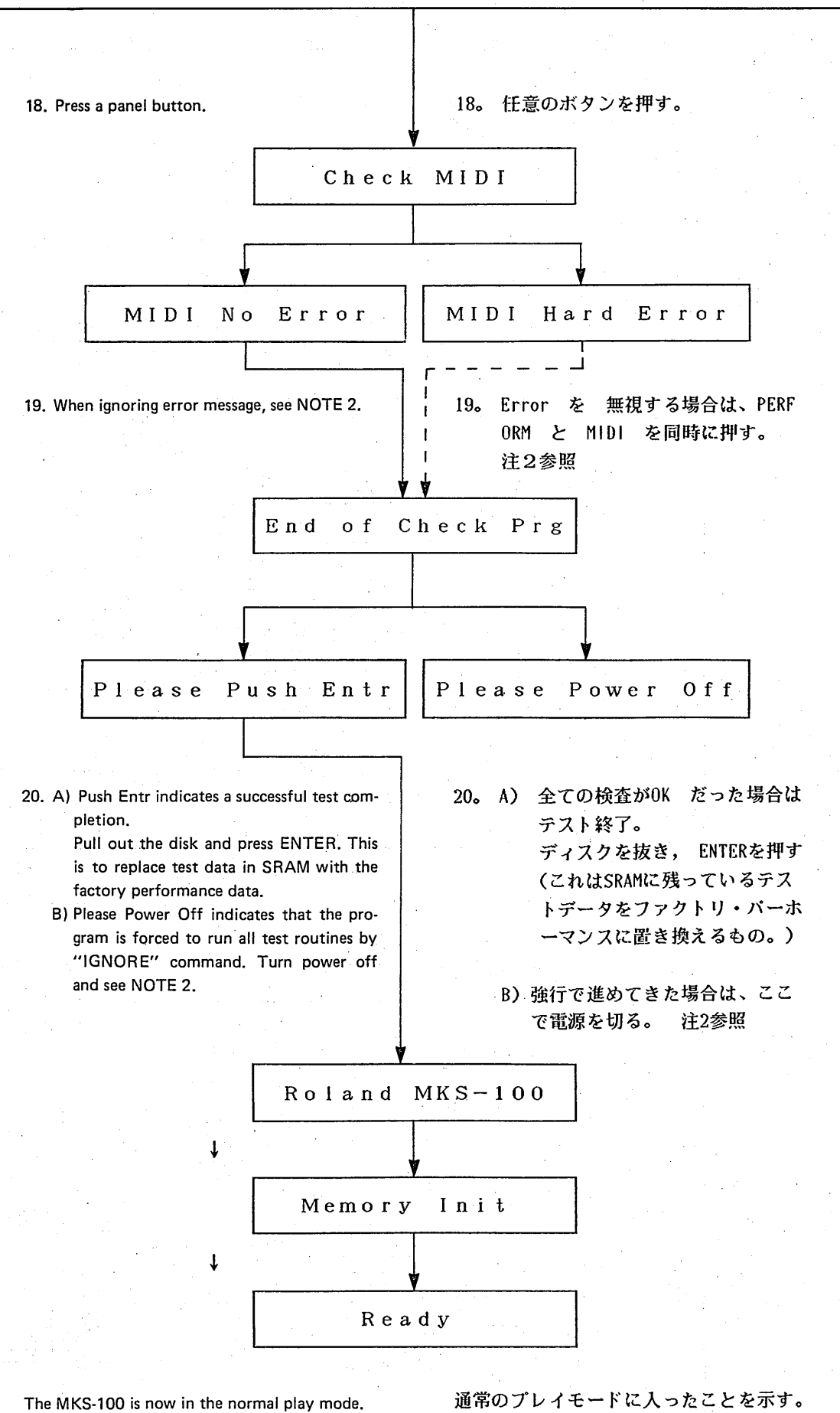
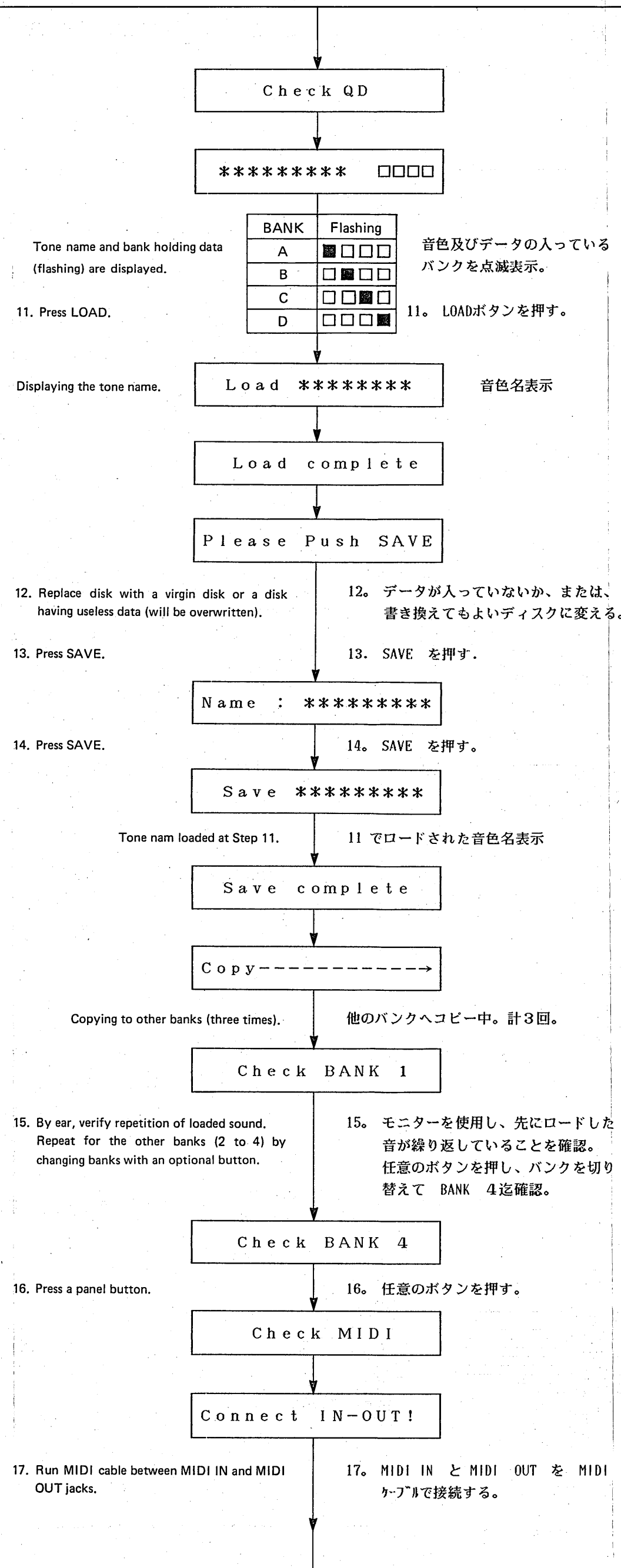
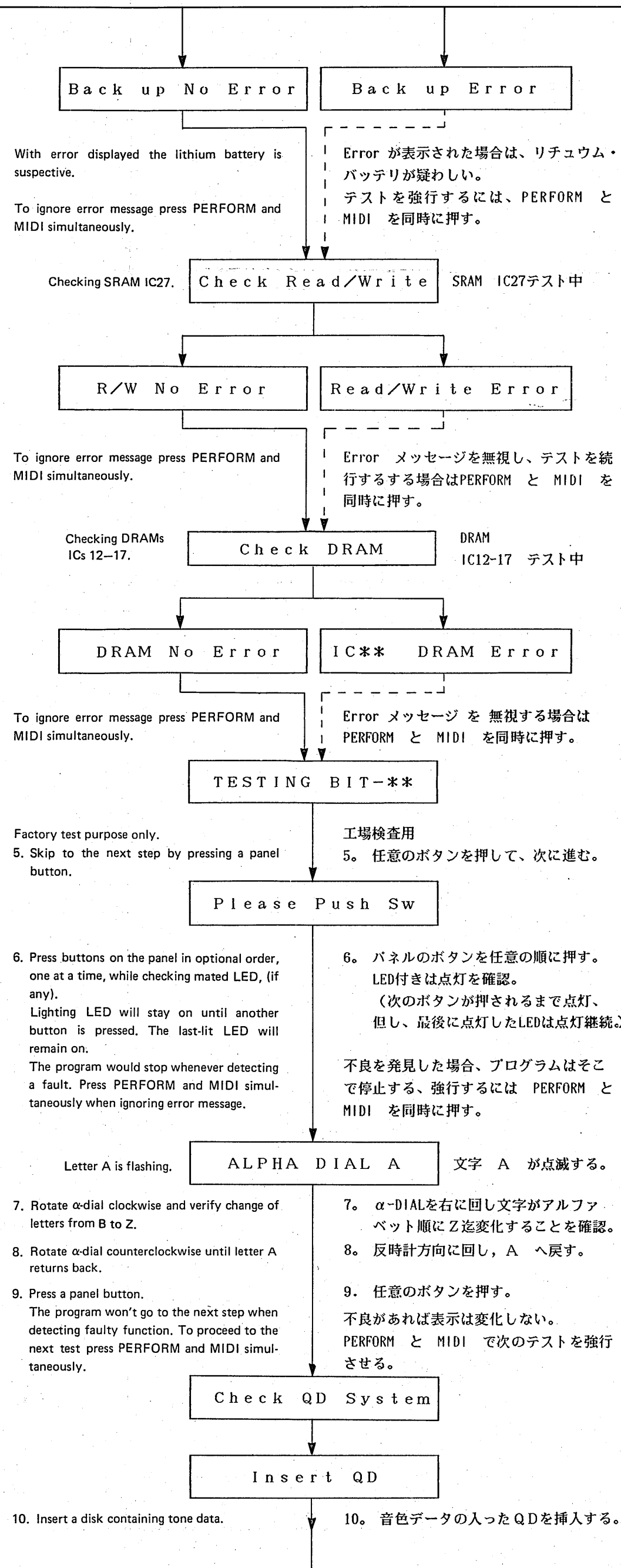
注.

異常を発見すると、プログラムは該当箇所、またはエラー・メッセージを表示したままで停止します。但し、PERFORMとMIDIボタンを同時に押すことにより、引き続き次のテストを強行させることが出来ます。

1. ROM(IC26)バージョン・ナンバー
2. メモリ・バックアップ (バッテリー)
3. S-RAM(IC27)
4. D-RAM(IC12-17)
5. IC10 (工場検査専用)
6. スイッチおよびLED
7. ロータリ・エンコーダ
8. QDドライブ
9. アウトプット
10. MIDI

テストモード

1. PERFORM と MIDIを押しながら電源を投入する。



NOTE 1

CPU compares data stored in the SRAM IC27 with the test data. Naturally both data are different with each other. During the next R/W routine the data to be tested is stored into the RAM.

NOTE 2

When the test is finished at this point, data generated during test routines are left in SRAM. In this case reapply the power while pressing down ENTER and the SRAM is refilled with the factory performance data (Initialization).

注1.

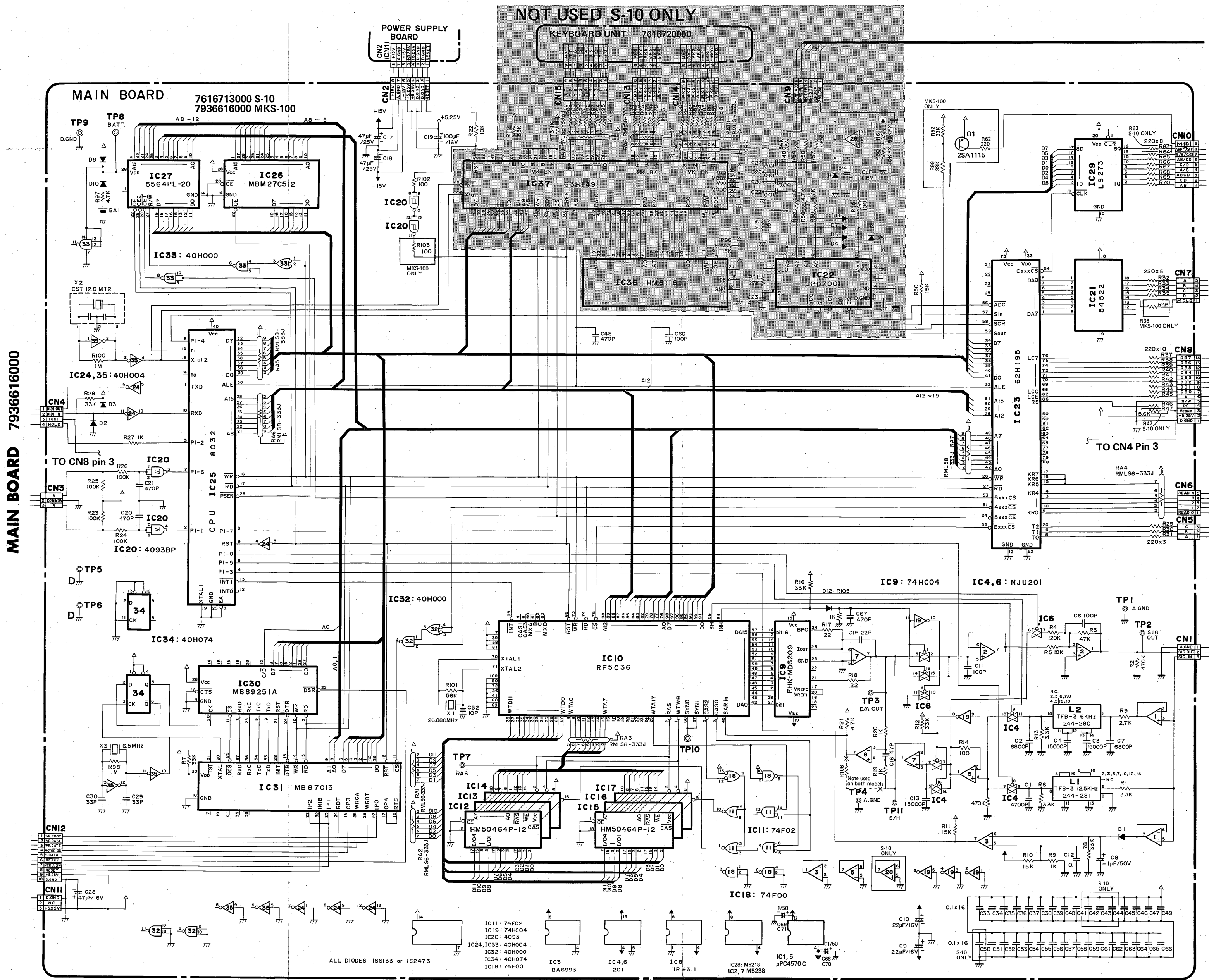
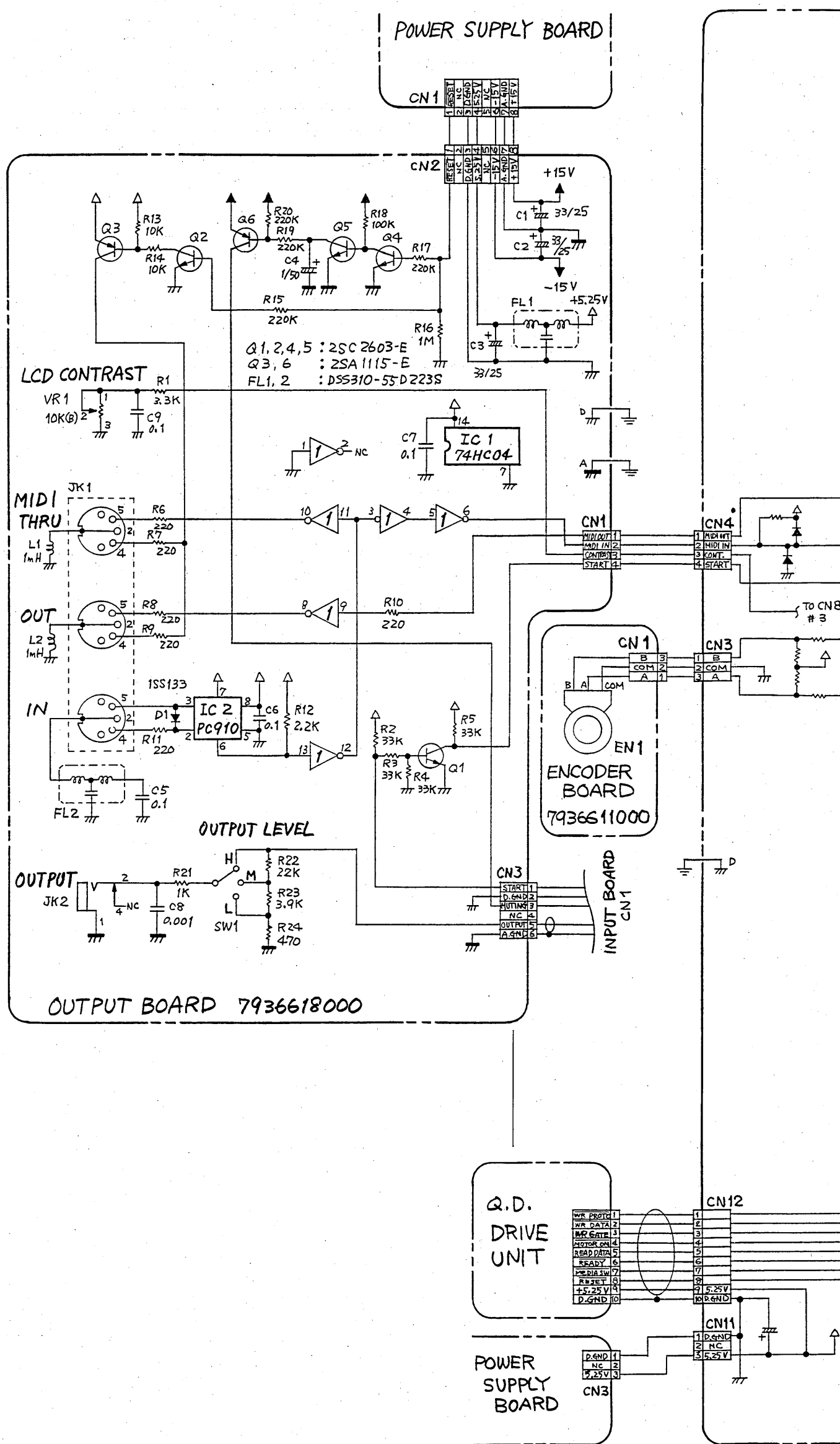
CPUはSRAM IC27 にバックアップされているデータと、SRAMテストデータを比較するが、この時点では一致しない。次のR/Wテストで、被テスト・データが書き込まれる。

注2.

この段階でテストを終了すると、SRAMにはテスト・データが残ったままととなる。一旦電源を切り、ENTERを押しながら再投入すると演奏用データ (ファクトリ・パフォーマンス・データ) がSRAMに転送される (SRAM イニシライゼーション)。

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62

CIRCUIT DIAGRAM



1234567891011121314151617181920212223242526272829303132333435363738

A

B

C

D

E

F

G

H

I

J

K

L

M

N

O

P

Q

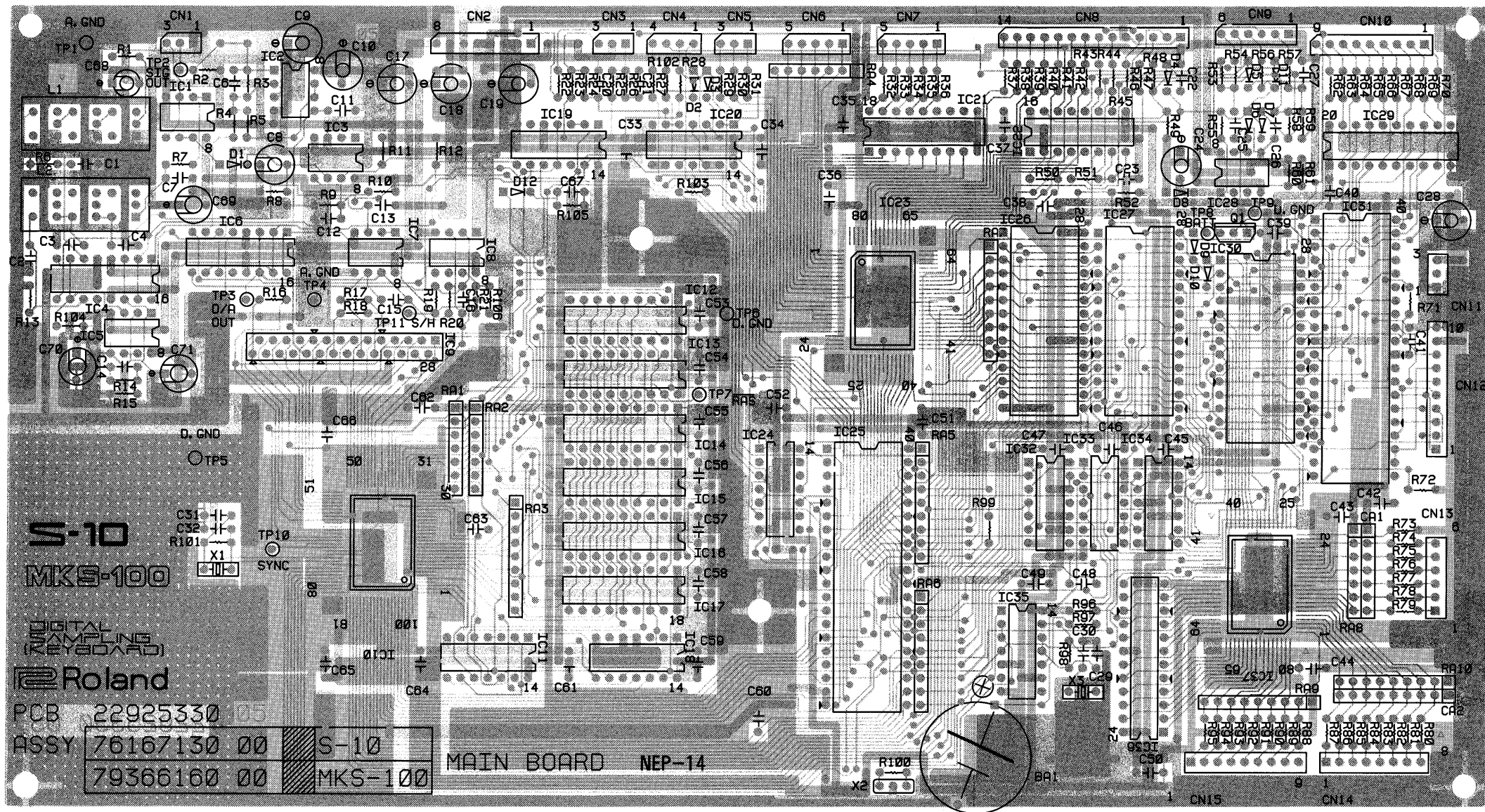
R

S

T

U

MAIN BOARD 7936616000 (pcb 22925330)



Replacement for IC1 and IC5 should be μ PC4570C only.
IC1またはIC5を交換する場合は、 μ PC4570Cのみを使用のこと。

ADVARSEL !
Lithiumbatteri. Eksplosionsfare.
Udskiftning må kun foretages af en sagkyndig,
og som beskrevet i servicemanual.

Lithium batteri må kun udskiftes med samme type
og fabrikat.

ADVARSEL !
Lithiumbatteri. Fare for eksplotion.
Ma bare skiftes af kvalifisert tekniker som
beskrevet i servicemanualen.

Lithium batteri må kun utskiftes med samme type
og fabrikat.

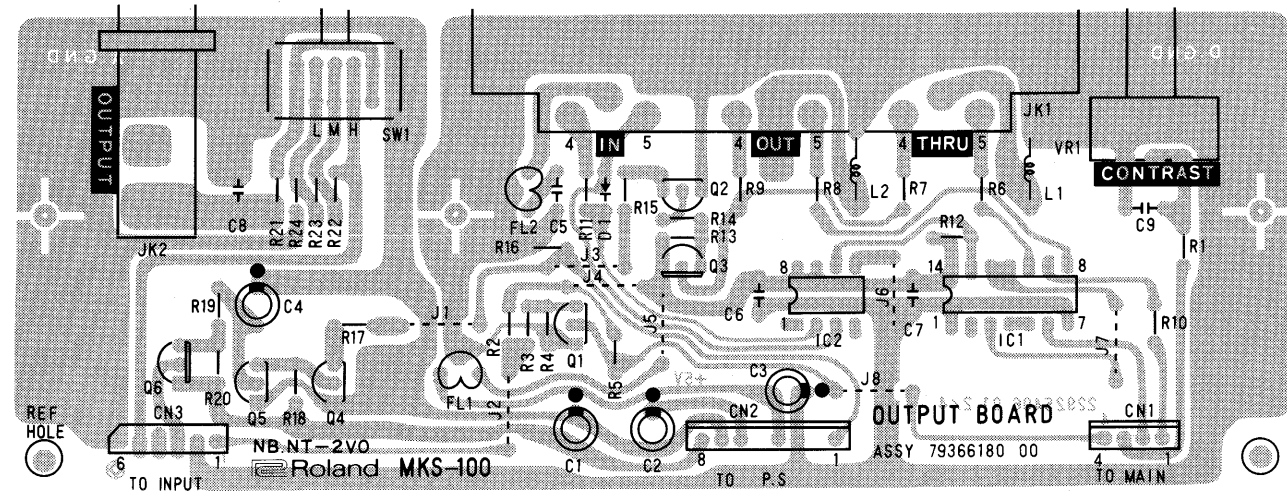
VARNING !
Lithiumbatteri. Explosionsrisk.
Får endast bytas av behörig servicetekniker.
Se instruktioner i servicemanualen.

Lithium batteri för endast ersättes med samme typ
och fabrikat.

VAROITUS !
Lithiumparisto. Räjähdysvaara.
Pariston saa vaihtaa ainoastaan
alan ammottimies.

Kun vaihat lithium pariston KÄYTÄ saman valmista-
jan samaa tyyppiä.

OUTPUT BOARD 79366180000 (pcb 2292540601 2/4)

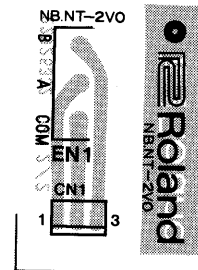


Compatibility – Main Board –
MKS-100 main board circuit is assembled on a PCB
numbered 22925330 that is also employed on Roland
keyboard sampler S-10. Having less components,
MKS-100 mian board can be replaced by an S-10's with
small component changes as shown below.
The reverse does not hold true . . . too may components
to be changed.

メインボードの互換性について
MKS-100とS-10は同じPCB(22925330)を使用していま
す。使用部品が一部異なるだけなので下表の通りわ
ずかな変更でS-10の基板をMKS-100用に改造する
ことが可能です。(MKS-100からS-10への変換は
変更部品点数が多いため避けた方が賢明)

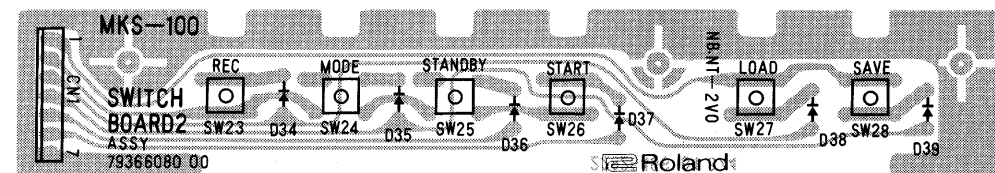
Required Modification On S-10 Main Board	
Add (追加)	Remove (削除)
Q1 2SA1115	R47 5.6K (CN8 pin 3)
R36 220 Ω (CN7 pin 1)	Replace (交換)
R52 33K (Q1 base)	IC26 with ROM P/N 15179798
R62 220 Ω (Q1–CN10 pin 7)	
R99 33K (Q1 base)	
R103 100 Ω (IC20 pin 11)	

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39

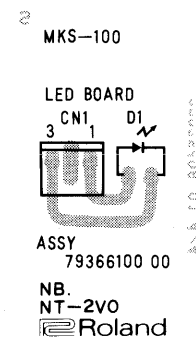
A
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O
P
Q
R
S
T
U
V

ENCODER BOARD
7936611000
 (pcb 22925332 2/2)

SWITCH BOARD 2
7936608000
 (pcb 2292540600 3/4)



LED BOARD
7936610000
 (pcb 2292540600 4/4)

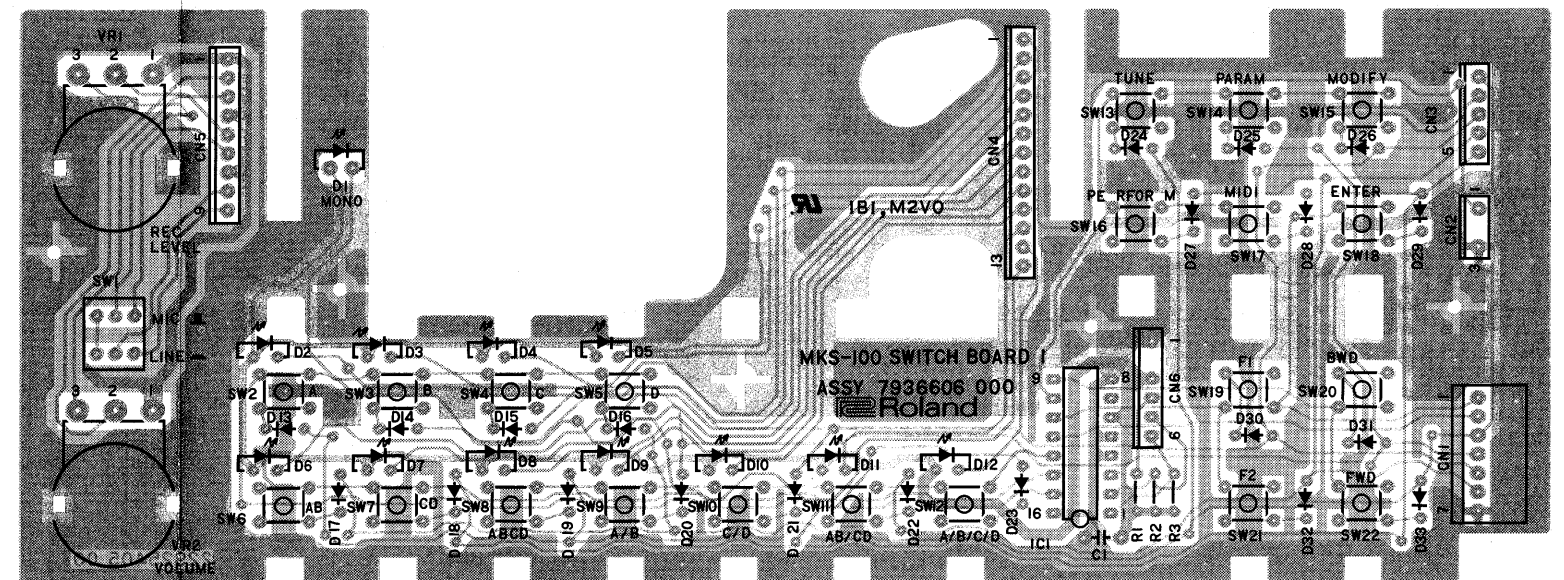


INPUT BOARD ICs 2-4

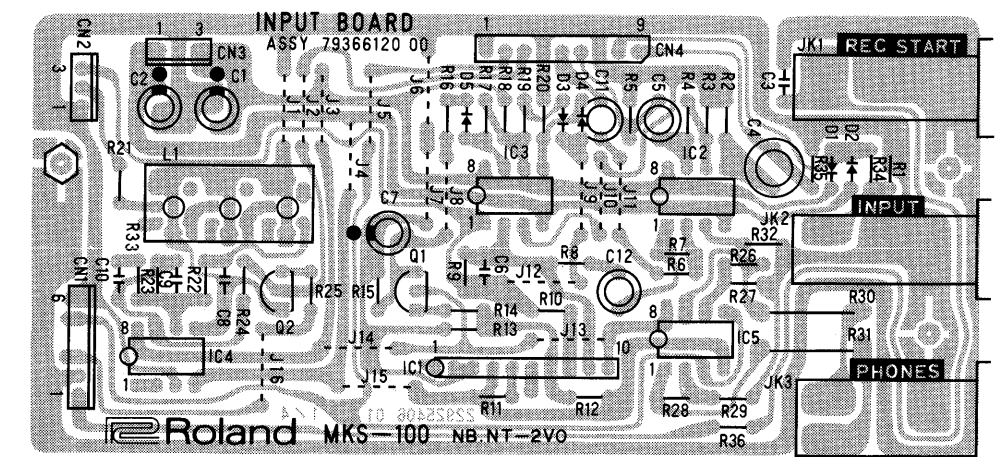
EFF SN	IC type used
700100-700149	NJM2068D-D
720150-720849	
730850-UP	μPC4570C

Replacement for ICs 2-4 should be μPC4570C only otherwise S/N ratio will become lowered.
 IC2-4を交換する場合は、μPC4570Cのみを使用。
 (S/N比向上のため)

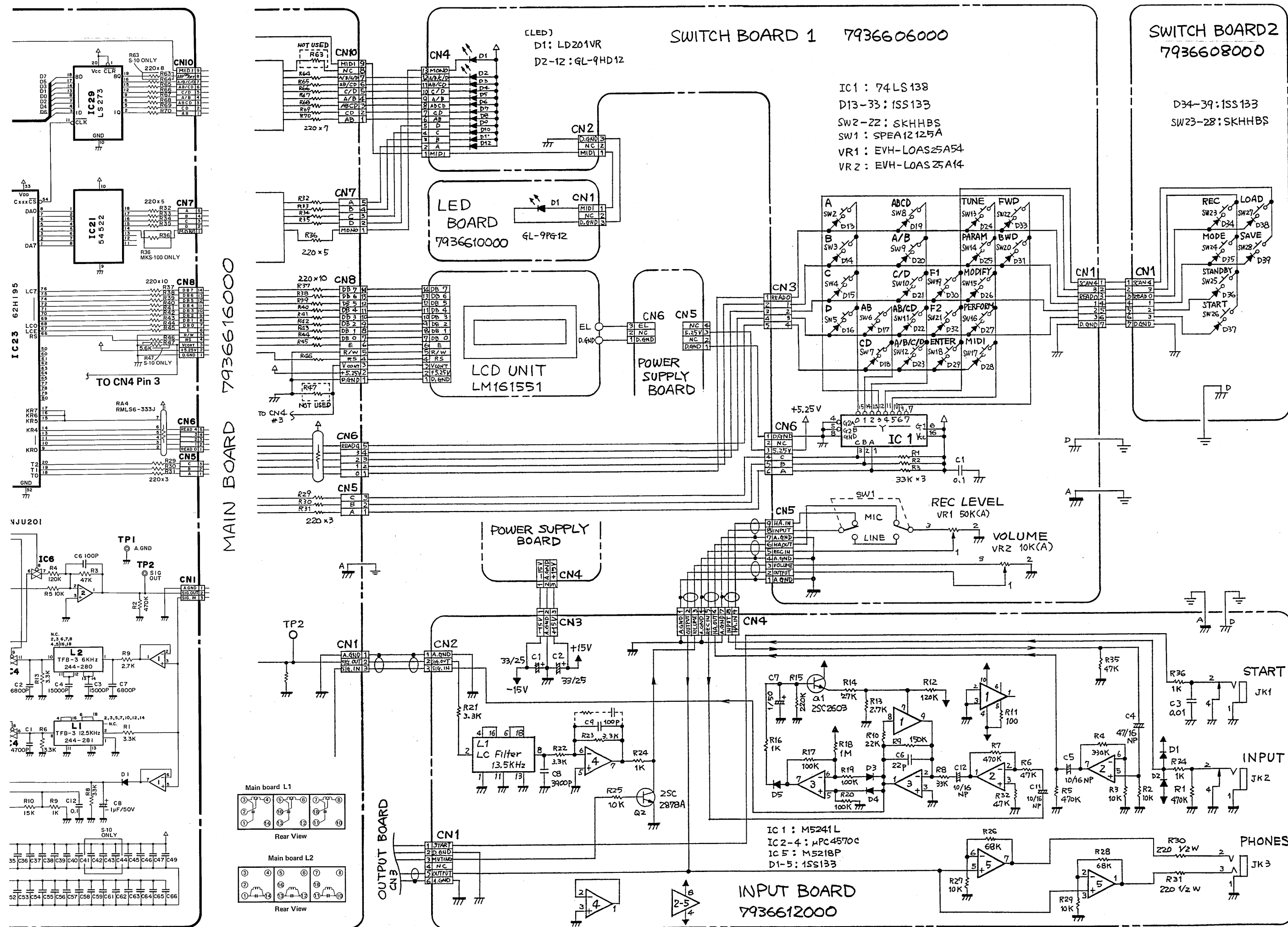
SWITCH BOARD 1
7936606000
 (pcb 2292540500)



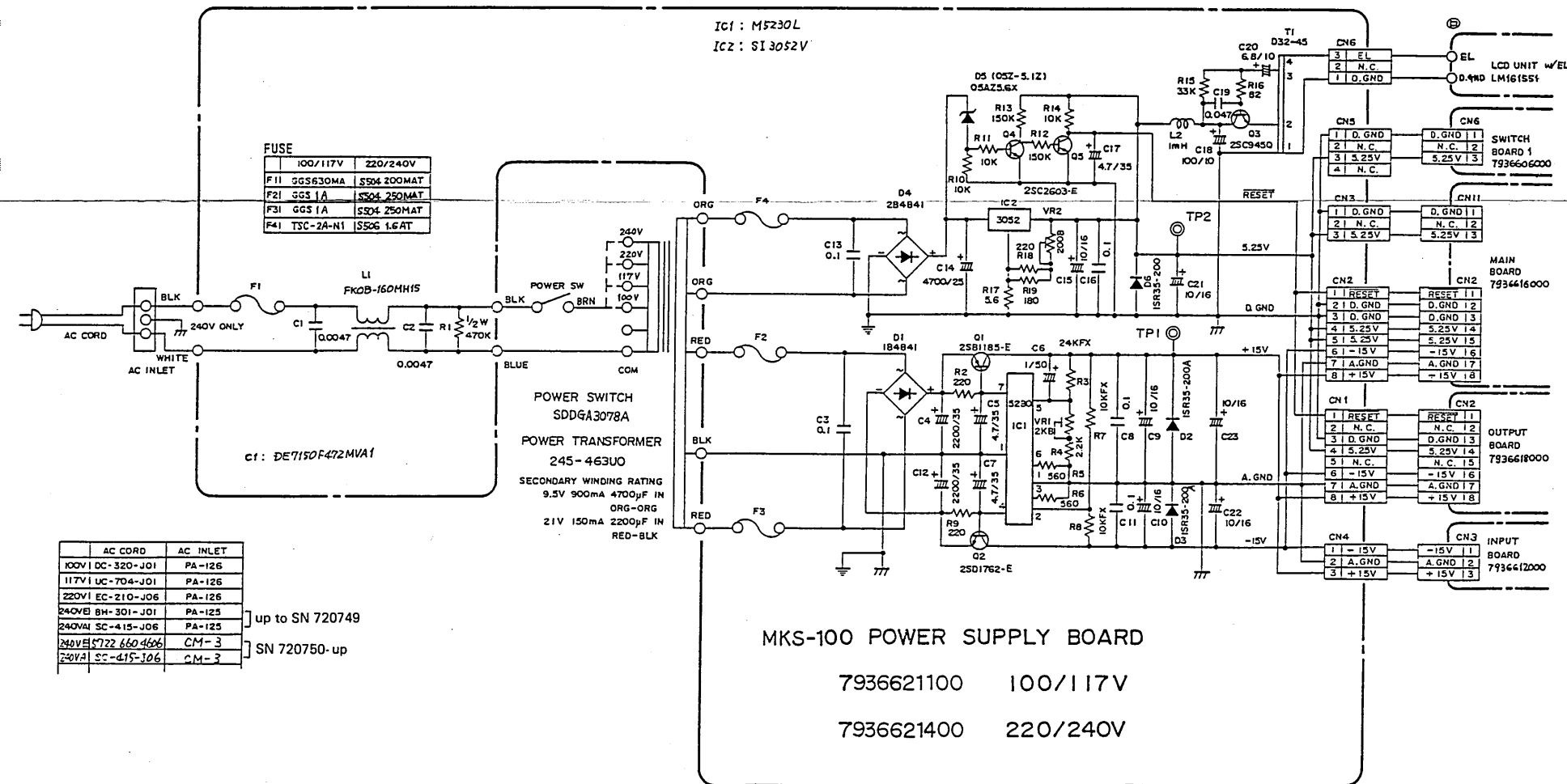
INPUT BOARD
7936612000
 (pcb 22925406000 1/4)



CIRCUIT DIAGRAM

A
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I
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K
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M
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O
P
Q
R
S
T
U
V
W
X
Y
Z

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48

A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P
Q
R
S
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U
V
W
X
Y
Z**Compatibility**

Any voltage version of MKS-100 Power Supply Board can work with S-10 and vice versa, provided that the following modifications are done.
Replace on-board heat sink and wirings with one existing on a given product. Change fuses as necessary.

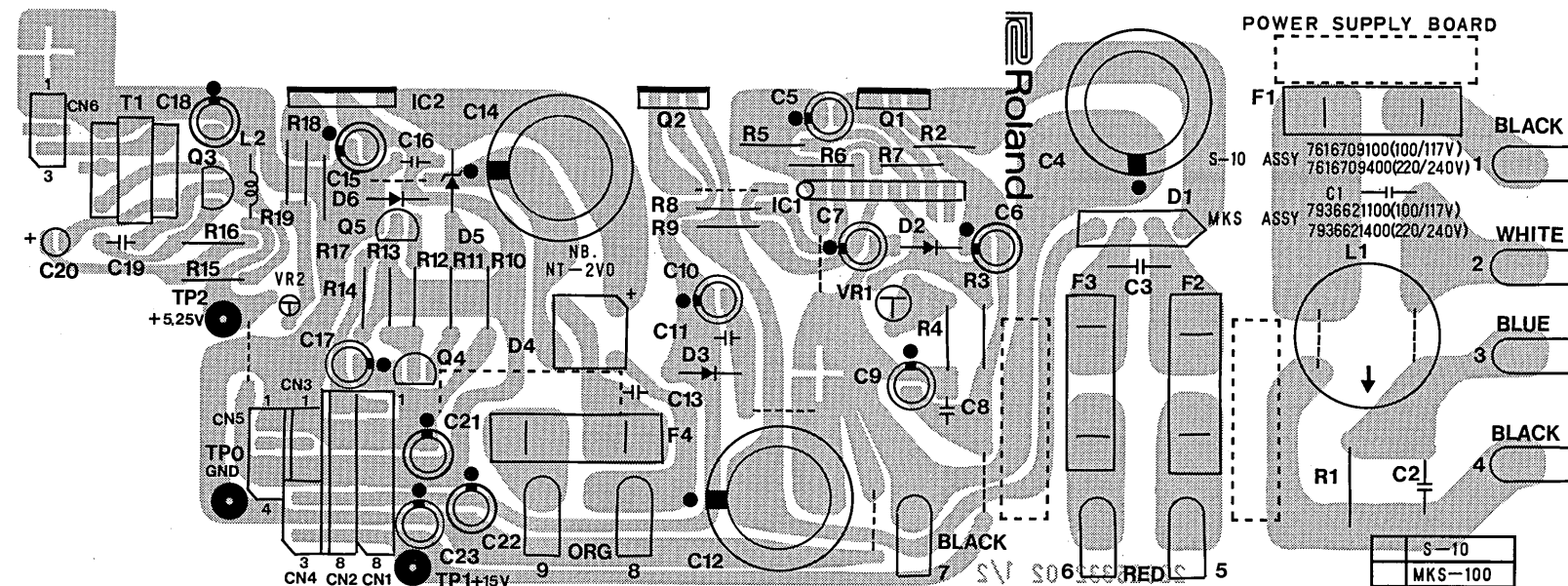
互換性について

MKS-100とS-10の電源基板は下記の変更を行なうことにより相互に使用可能となります。
補修基板上のヒートシンクおよびワイヤリングを製品で使用中的ものに取り換える。
電圧が異なっている場合はヒューズも交換する。

POWER SUPPLY BOARD

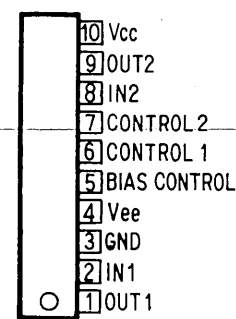
7936621100 (pcb 22925332 1/2) 100/117V

7936621400 (pcb 22925332 1/2) 220/240V

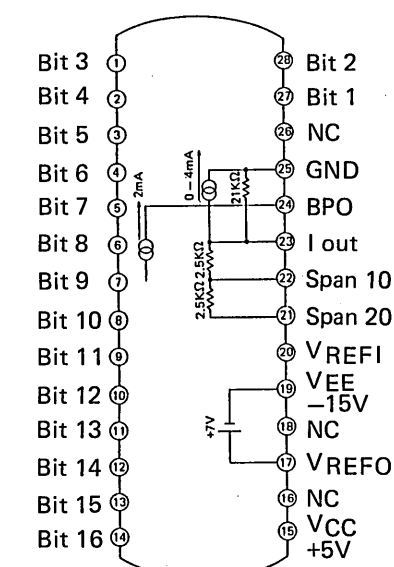
**IC DATA****VCA**

5241L

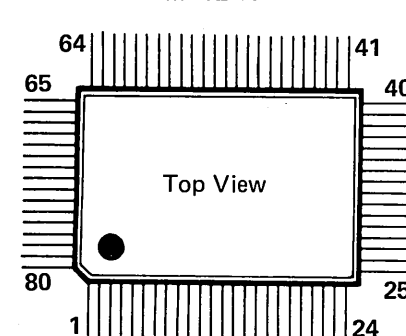
Top View

**EHK-MD6209 D/A CONVERTER**

Top View



MB62H195

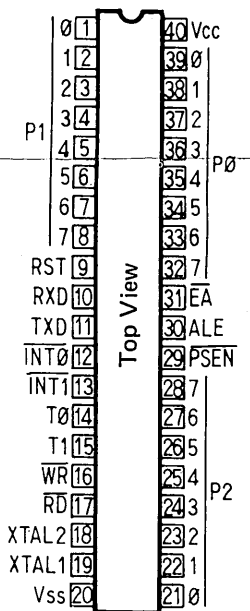
**I/O GATE ARREY**

No	I/O	NAME	No	I/O	NAME	No	I/O	NAME	No	I/O	NAME
1	O	DA7	21	O	T3	41	I/O	D0	61	O	D10
2	O	DA6	22	O	T4	42	O	A0	62	O	DC2
3	O	DA5	23	-	NC	43	O	A1	63	-	NC
4	O	DA4	24	O	5xxxCS	44	O	A2	64	O	DC1
5	O	DA3	25	O	LED	45	O	A3	65	O	DC0
6	O	DA2	26	I	WR	46	O	A4	66	O	RS
7	O	DA1	27	I	RD	47	O	A5	67	O	LCE
8	O	DA0	28	I	A12	48	O	A6	68	O	LCO
9	I	KR0	29	I	A13	49	O	A7	69	O	LC1
10	I	KR1	30	I	A14	50	O	ROM	70	O	LC2
11	I	KR2	31	I	A15	51	O	4xxxCS	71	O	LC3
12	-	GND	32	I	A16	52	-	GND	72	O	LC4
13	I	KR3	33	-	VDD	53	O	6xxxCS	73	-	VCC
14	I	KR4	34	I/O	D7	54	O	CxxxCS	74	O	LC5
15	I	KR5	35	I/O	D6	55	O	OUT0	75	O	LC6
16	I	KR6	36	I/O	D5	56	O	ADC	76	O	LC7
17	I	KR7	37	I/O	D4	57	I	Sin	77	O	DA11
18	O	T0	38	I/O	D3	58	O	SCR	78	O	DA10
19	O	T1	39	I/O	D2	59	O	Sout	79	O	DA9
20	O	T2	40	I/O	D1	60	O	D11	80	O	DA8

CPU

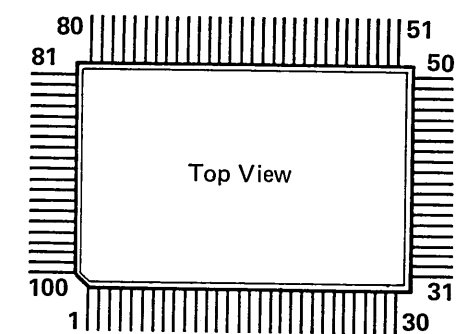
8032

Top View



RF5C36

Top View

**SAMPLER CUSTOM IC**

PIN No	PIN NAME	I/O	PIN No	PIN NAME	I/O
1	WTWR	O	51	DA9	O
2	RAS	O	52	DA10	O
3	CAS0	O	53	DA11	O
4	CAS1	O	54	DA12	O
5	CAS2	O	55	DA13	O
6	CAS3	-	56	DA14	O
7	VCC	O	57	DA15	O
8	WTA0	O	58	VCC	-
9	WTA1	O	59	SH	O
10	WTA2	O	60	MXA	O
11	WTA3	O	61	MXB	O
12	WTA4	O	62	MXC	O
13	WTA5	O	63	MXD	O
14	WTA6	O	64	INH	O
15	WTA7	O	65	RST	I
16	WTA8	O (NC)	66	SYNO	O
17	WTA9	O (NC)	67	SYN1	I
18	WTA10	O (NC)	68	TEST2	I
19	WTA11	O (NC)	69	TEST1	I
20	WTA12	O (NC)	70	XTAL1	XIN
21	WTA13	O (NC)	71	XTAL2	XOUT
22	WTA14	O (NC)	72	TESTCK	I
23	WTA15	O (NC)	73	WR	I
24	WTA16	O (NC)	74	RD	I
25	WTA17	O	75	CS	I
26	GND	-	76	A0	I
27	WTD0	I/O	77	A1	I
28	WTD1	I/O	78	A2	I
29	WTD2	I/O	79	A3	I
30	WTD3	I/O	80	GND	-
31	WTD4	I/O	81	VCC	-
32	WTD5	I/O	82	A4	I
33	WTD6	I/O	83	A5	I
34	WTD7	I/O	84	A6	I
35	WTD8	I/O	85	A7	I
36	WTD9	I/O	86	A8	I
37	WTD10	I/O	87	A9	I
38	WTD11	I/O	88	A10	I
39	VCC	-	89	A11	I
40	SARin	I	90	A12	I
41	GND	-	91	DB0	I/O
42	DA0	O	92	DB1	I/O
43	DA1	O	93	DB2	I/O
44	DA2	O	94	DB3	I/O
45	DA3	O	95	DB4	I/O
46	DA4	O	96	DB5	I/O
47	DA5	O	97	DB6	I/O
48	DA6	O	98	DB7	I/O
49	DA7	O	99	INT	O
50	DA8	O	100	GND	-

* XIN, XOUT : crystal

* OUTPUT LOAD CONDITION : CL=100pF

CHANGE INFORMATION

変更案内

Software Revisions (IC26 Main Board)

ROMバージョンアップ

ROM Ver. No. EFF. SN	DESCRIPTION	改良点
Ver. 1.02 700115 700149	Quick repetition of a note results in clicks due to DC drift. Ver. 1.02 eliminates the problem by assigning different module to each NOTE ON.	同一音が連打されると、DC変動による異音が発生した、NOTE ON 毎に異ったモジュールがアサインされる様にする。
Ver. 1.04 700100 700114 720150	Feeding GATE inputs equal to or more than the number of voices in EXT GATE PLAY mode silences the voices for the time set by TRG G-TIME. Ver. 1.04 cures this problem.	EXT GATEPLAY モードにおいて、ボイスの数以上のゲート入力加わると、TRIG G-TIMEで設定された時間不鳴りとなった。

Hardware Improvements

回路

EFF SN 実施製番	MAIN BOARD			INPUT BOARD	OUTPUT BOARD	
	PCB No. (etched) PCB No. (パターン側)	D12, C67 R105	IC1 IC5	IC2, IC3, IC4	L1, L2	R12
700100-700149	22925330 02	*1 surface mounted on foil side 裏付	NJM2068D-D	NJM2068D-D	On 220V Version only (surface mounted)	10K
720150-720849	22925330 03				On all Versions (surface mounted)	*3 2.2K
730850-731649	22925330 04	Component side 部品側	*2 uPC4570C	*2 uPC4570C	On all Versions (component side)	
741650-UP	22925330 05					

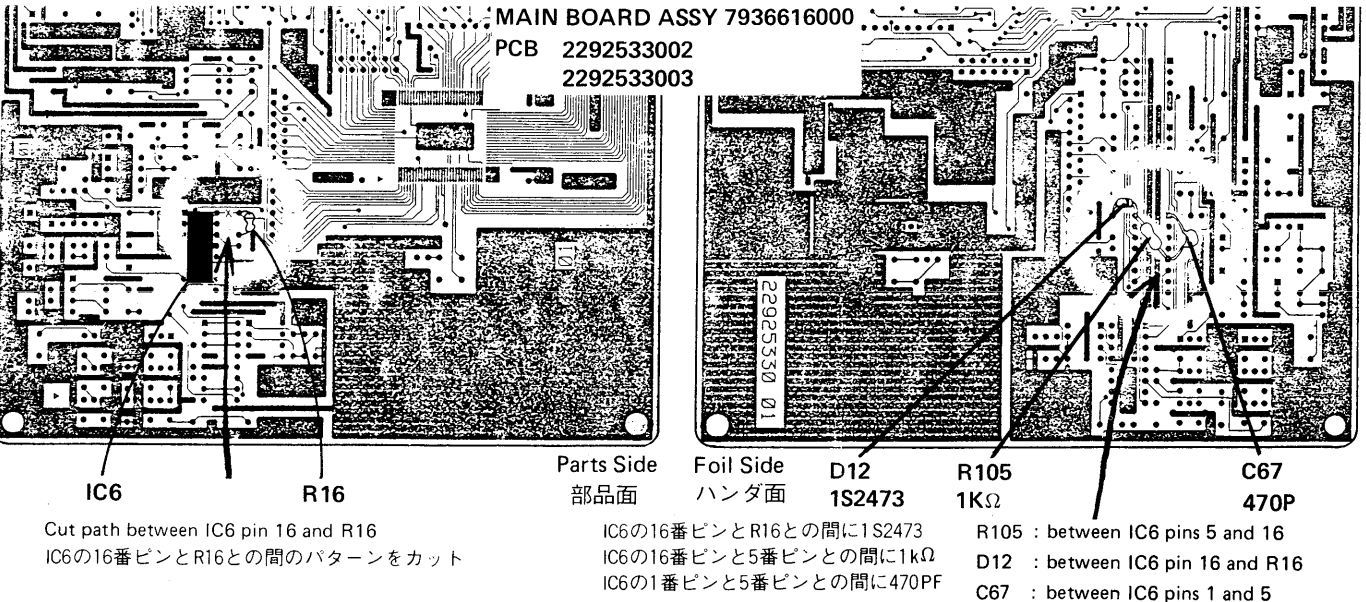
- *1 Add these parts between IC10 (INH) and IC6 (pins 1, 16) as shown below. This will fatten INH pulse and improve S/N ratio during ENV release.

*2 To increase S/N ratio. Use μ PC4570C only, when replacing. Also capacitor $1\mu/50V$ (C68-C71) is connected to DC power source of these ICs (pins 4 and 8).

*3 To quicken response to MIDI IN.
- *1 IC10のINHピンとIC6のピン1、16間に挿入、下図参照。INHのパルス巾を広げENVリリース時のノイズを軽減。

*2 SN比改良のため。補修用は μ PC4570に限る。なお、これらICのピン4と8にもノイズ軽減のため、 $1\mu/50V$ を追加(C68-71)。

*3 MIDI入力に対する応答時間を縮めるため。



CHECKING AND ADJUSTING

点検および調整

NOTE
Running Diagnostic Programsdescribed on page 9 before any service will help fault isolation.

1. Power Supply

Instrument required . . .Digital voltmeter having 1mV resolution. Connect GND to TP-0 of power supply board.

Lithium Battery

With power off determine the voltage on TP-8 of main board. It must be more than 2.7V for positive memory backup.
- 1.電源

接続

測定器 — デジボル 分解能1mV以上

GNDを電源基板のTP-0に接続する。

リチウムバッテリー

電源オフの状態、メイン基板上のTP-8の電圧を測定。2.7V以上であること。

- +15V

Turn the switch on. Connect the meter to TP-1 of power supply board. Adjust VR1 of power supply board for a +15 $\pm$ 0.1V reading.

-15V

Verify that the voltage on the D3 anode is -15 $\pm$ 0.4V.

+5.25V

Connect the meter to TP-2 of power supply board. Adjust VR2 for +5.25 $\pm$ 0.005V reading.
- +15V

電源をオンする。

電源基板のTP-1にデジボルを接続。VR1で +15 $\pm$ 0.1Vに調整する

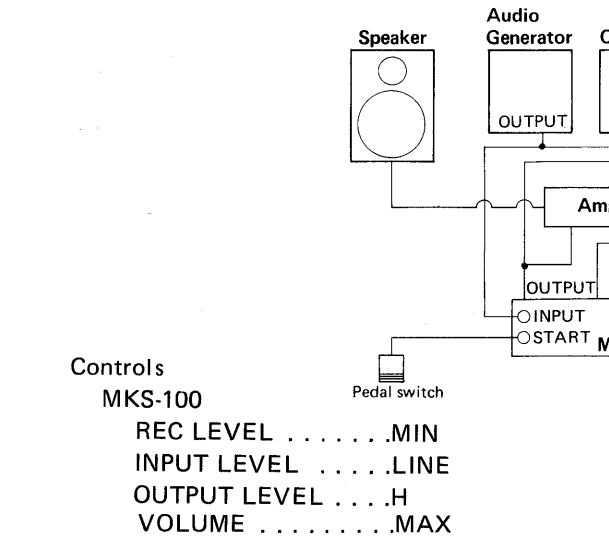
-15V

D3アノードの電圧が、-15 $\pm$ 0.4Vであることを確認する。

+5.25V

電源基板のTP-2にデジボルを接続する。
+5.25 $\pm$ 0.005VになるようVR2を調整する。

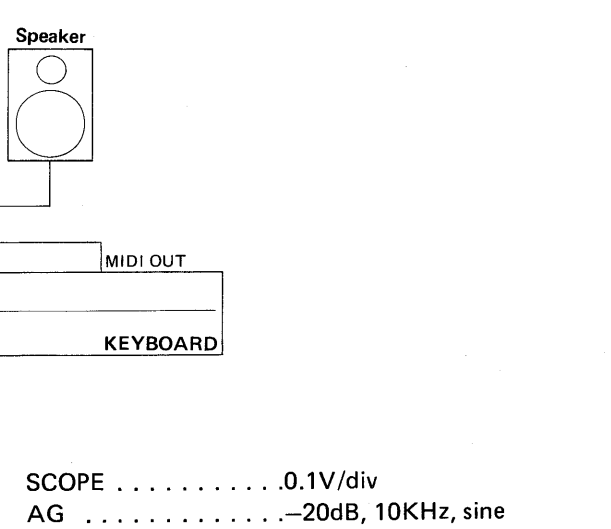
2. REC Setup



2-1. Level Meter
Press buttons in the order of A, REC and STAND-BY. Verify that the LCD shows the minimum level.



2. REC 接続



2-1. レベルメータ
ボタンをA、REC、STANBYの順で押す。
LCDのレベル指示が最低のまま動かないことを確認する。



2-2. Output Level

Adjust REC LEVEL for 0.56 Vp-p $\pm$ 15% reading at OUTPUT jack.

Verify the level change at different OUTPUT LEVEL settings:

M 0.092 Vp-p $\pm$ 15%
L 0.010 Vp-p $\pm$ 15%

2-3. Input Level

Set AG output to -5dB.

Set INPUT LEVEL to MIC.

Verify the 0.56 Vp-p $\pm$ 15% at OUTPUT jack.

Leave the settings unchanged for the next step.

2-4. Filter

Press MODE and FWD. LCD will read.

SMP CLK = 30 kHz

The 10KHz, sine must be at OUTPUT jack.

Using α -dial set sampling clock to 15KHz and verify missing 10KHz signal.

Lower the input frequency to 1KHz and verify 1KHz at OUTPUT jack.

2-5. Start Jack

Set A.G. to -20dB, 10KHz, sine.

Start recording with the pedal.

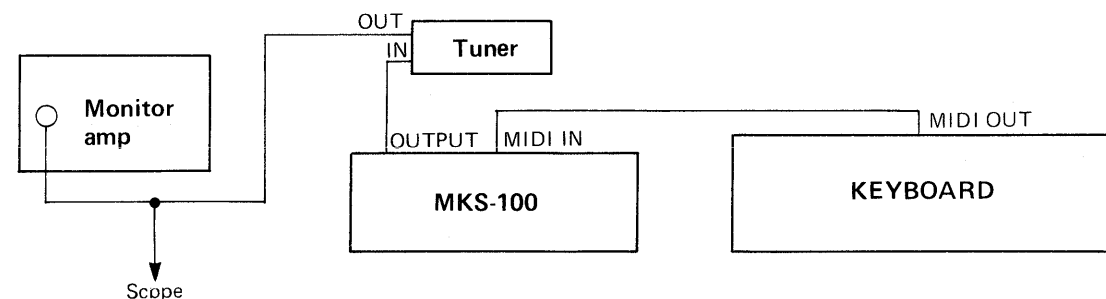
2-6. REC Key

Press middle C (C4) and verify 10KHz signal at OUTPUT jack.

The output must be at 5KHz when C3 key is played.

3. TUNE

Setup



Record 442Hz sine into a QD. Load this QD.

Play A4 key (above middle C) and verify a 442Hz $\pm$ 1% output with the waveform as shown below.

2-2. アウトプット・レベル

OUTPUTジャックにおけるレベルが 0.56Vp-p

$\pm$ 15%になるようREC LEVELを調整する。

OUTPUT LEVELを切り替えた時の出力がは下記の値であること。

M = 0.092 Vp-p $\pm$ 15%
L = 0.010 Vp-p $\pm$ 15%

2-3. インプット・レベル

発振器の出力を -50dB に設定する。

INPUT LEVEL を MIC に設定する。

OUTPUTジャックからの出力は、0.56Vp-p $\pm$ 15%であること。

このままの状態、2-4へ進む。

2-4. フィルタ

MODE、次に FWD を押す。LCDには、

SMP CLK = 30 kHz

が表示される。

OUTPUT ジャックからは、10KHzが出力される。

サンプリング・クロックを15KHzに設定し10KHzが出力されていないことを確認。

発振器を1kHzに設定する。1kHzのサイン波が出力されることを確認。

2-5. スタート・ジャック

発振器を-20dB, 10KHz, サインに設定。

ペダルスイッチでレコーディングがスタートすることを確認。

2-6. REC KEY

C4キー（中央C）を弾き、10KHzのサイン波が出力されることを確認。

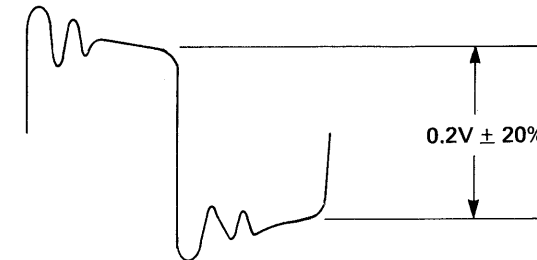
C3キーを弾く、出力は5KHzとなること。

3. チューン

接続

442Hzの矩形波を録音してあるQDをロードする。

A4（中央Cの上）キーを押す。出力は下図の様な波形でかつ442Hz $\pm$ 1%であることを確認。



4. ARPEGGIO

Press F2 then PERFORM. Turn Arpeggio on with α -dial. Press C, E and G keys and verify repetition of these signals on OUTPUT jack.

5. EXT Gate Play

Press PERFORM. Press FWD until display shows

Ext Gate Play

Press F1

— — — —

Set INPUT LEVEL to MIC and REC LEVEL to MIN.

Set AG to -50dB, 10kHz, sine.

Rotate α -dial to show a key note (C1 to G7).

Make sure that the note displayed becomes audible as REC LEVEL is turned clockwise.

6. NOISE LEVEL

Connect a noise meter to OUTPUT jack.

Set MKS-100 controls as follows:

OUTPUT LEVEL H
INPUT LEVEL LINE
VOLUME MAX
REC LEVEL MIN

Load the QD containing a 442Hz square wave.

Press buttons in the order of F1, REC MODE, FWD and FWD.

Press button F1, REC, MODE FWD and FWD in that order.

Using α -dial, select REC TRIG MANUAL.

Press START twice.

Verify S/N ratio of less than -85dB.

Press C4 key and verify S/N ratio of less than -80dB.

4. アルペジオ

ボタンF2、続けて PERFORM を押す。

α -DIAL で ARPEGGIO を オン にする。

C, E, Gのキーを押し、これらの音が順次繰り返されることを確認。

5. EXTゲート・プレイ

設定

発振器 -50dB, 10kHz, sine

MKS-100

INPUT LEVEL -- MIC: REC LEVEL -- MIN

PERFORMを押す。下図の表示が出るまでFWDを押す。

Ext Gate Play

F1を押す。

— — — —

が表示される。

α -DIALでキーノート（C1-G7）を表示させる。

REC LEVELを右に回して行くと、表示されている音が出力されることを確認。

6. ノイズレベル

ノイズ・メータを OUTPUT ジャックに接続

設定

MKS-100

OUTPUT LEVEL ----- H

INPUT LEVEL ----- LINE

VOLUME ----- MAX

REC LEVEL ----- MIN

442Hzの矩形波を録音してあるQDをロードする。

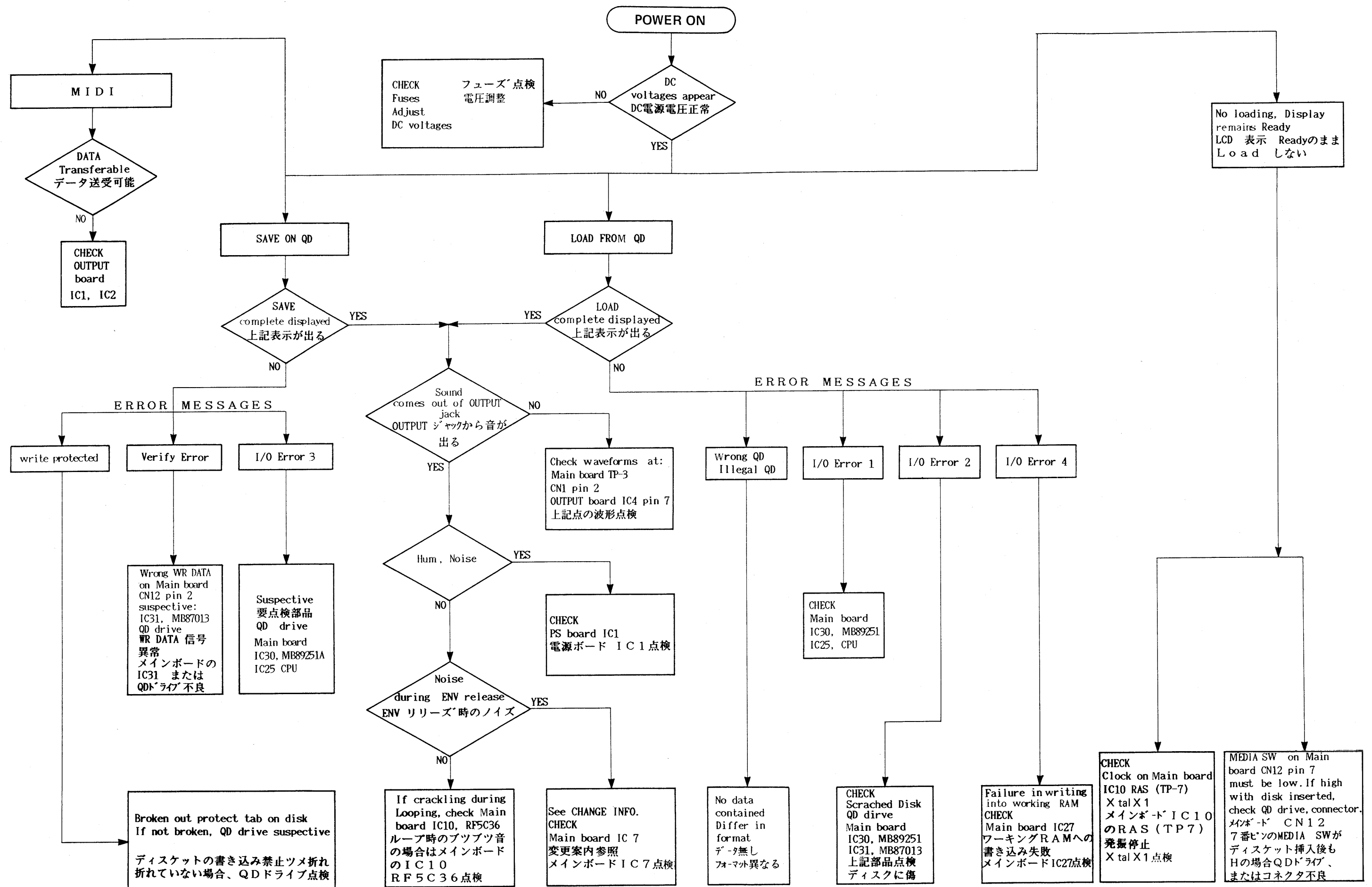
ボタン F1, REC, MODE, FWD, FWDを順番に押す。

α -DIAL で REC TRIG を MANUAL に設定。STARTを2回押す。

S/N比が -85dB以下であることを確認。

C4キーを押す。S/N比は-80dB以下であること。

TROUBLESHOOTING トラブルシューティング



MIDI IMPLEMENTATION

8-voice digital sampling module

Status	Second	Third	Description	
1011 nnnn	0000 0110	0vvv vvvv	Data Entry MSB	*1-1,2
1011 nnnn	0010 0110	0vvv vvvv	Data Entry LSB	*1-1,2
1011 nnnn	0110 0100	0vvv vvvv	RPC LSB	*1-1,2
1011 nnnn	0110 0101	0vvv vvvv	RPC MSB	*1-1,2
			RPC # = 0, 1	
1100 nnnn	0ppp pppp		Program Change	*1-1,3
			pppppp = 0 - 122	
1111 0000		1111 0111	System exclusive	*1-1,4

Notes :

*1-1 Transmitted if the corresponding function switch is ON.

*1-2 When BEND RANGE or MASTER TUNE is changed, RPC (Registered parameter control number) and its value are sent as follows.

RPC #	value MSB	value LSB	Description
0	0vvv vvvv	0000 0000	(Pitch bend sensitivity) BEND RANGE 0-12 semitone, 1 semitone step
1	0vvv vvvv	0vvv vvvv	(Master fine tuning) MASTER TUNE -99 - +99 cent, 1 cent step

*1-3 Program change number indicates the condition of the 'Sampling Structure'. (See Owner's manual)

*1-4 See section 3 (EXCLUSIVE COMMUNICATION).

Status	Second	Third	Description	
1000 nnnn	0kkk kkkk	0vvv vvvv	Note OFF, velocity ignored	
1001 nnnn	0kkk kkkk	0000 0000	Note OFF	
			kkkkkk = 24 - 103	*2-1
1001 nnnn	0kkk kkkk	0vvv vvvv	Note ON	
			kkkkkk = 24 - 103	*2-1
			vvvvvv = 1 - 127	
1011 nnnn	0000 0001	0vvv vvvv	Modulation depth	*2-2,3
1011 nnnn	0000 0110	0vvv vvvv	Data Entry MSB	*2-2,4
1011 nnnn	0010 0110	0vvv vvvv	Data Entry LSB	*2-2,4
1011 nnnn	0100 0000	0vvv vvvv	Hold1 OFF	*2-2
			vvvvvv = 0 - 63	
1011 nnnn	0100 0000	0vvv vvvv	Hold1 ON	*2-2
			vvvvvv = 64 - 127	
1011 nnnn	0110 0100	0vvv vvvv	RPC LSB	*2-2,4
1011 nnnn	0110 0101	0vvv vvvv	RPC MSB	*2-2,4
1100 nnnn	0ppp pppp		Program Change	*2-2,5
			pppppp = 0 - 127	
1110 nnnn	0vvv vvvv	0vvv vvvv	Pitch Bend Change	*2-2
1011 nnnn	0111 1011	0000 0000	ALL NOTES OFF	*2-6,7
1011 nnnn	0111 1100	0000 0000	OMNI OFF	*2-6
1011 nnnn	0111 1101	0000 0000	OMNI ON	*2-6
1011 nnnn	0111 1110	0000 0000	MONO ON	*2-6
1011 nnnn	0111 1111	0000 0000	POLY ON	*2-6
1111 0000		1111 0111	System exclusive	*2-2,8

Notes :

*2-1 Note numbers outside the range 24 - 103 are ignored.

*2-2 Received if the corresponding function switch is ON.

*2-3 vvvvvv = 0 : modulation OFF
vvvvvv = 1 - 127 : modulation ON (Depth ignored.)

*2-4 RPC and value (Data Entry) are recognized as follows.

RPC #	value MSB	value LSB	Description
0	0vvv vvvv	0xxx xxxx	BEND RANGE (0-12 semitone, 1 semitone step) xxxxxx is ignored.
1	0vvv vvvv	0vvv vvvv	MASTER TUNE (-99 - +99 cent, 1 cent step)

*2-5 Program number corresponds to the condition of the 'Sampling Structure'. (See Owner's manual)

*2-6 Mode Messages (123-127) are recognized also as ALL NOTES OFF. OMNI ON/OFF Messages are ignored.

MONO channel range 'mmmm' is recognized as follows.

1) 8-module mode (Normal, Velocity switch)

mmmm	True MONO channel range
0	8
1 - 8	1 - 8
9 - 127	8
Manual set	8

2) 4-module mode (Detune, Delay, Dual Tone, Velocity-Mix)

mmmm	True MONO channel range
0	4
1 - 4	1 - 4
5 - 127	4
Manual set	4

In MONO mode, channel of recognized each message is as follows.

message	'BASIC'	'GLOBAL'
Note on/off	individual	individual
Control change	basic	global
Mode message	basic	basic
Program change	basic	global
Pitch bender	individual	individual
Exclusive	basic	basic

* Global channel is equal to "basic channel - 1".
And if basic channel is 1, global channel is 16.

*2-7 Ignored in MONO mode.

*2-8 See section 3 (EXCLUSIVE COMMUNICATION).

3. EXCLUSIVE COMMUNICATION

It is possible to communicate with exclusive messages, in NORMAL MODE and SAMPLE DATA DUMP MODE.

NORMAL MODE, in which it is possible to play and generate sound, is explained in section 4, 5.

SAMPLE DATA DUMP MODE has following 4 functions explained in section 6-9.

When 'F1' and 'MIDI' buttons are pressed, it becomes SAMPLE DATA DUMP MODE, and LCD shows "Sample Data Xst". It means "ONE WAY SAMPLE DATA TRANSMIT".

Then 'FORWARD' button is pressed, LCD shows "Sample Data Xst". It means "HANDSHAKE SAMPLE DATA TRANSMIT".

Then 'FORWARD' button is pressed, LCD shows "Sample Data Rcv". It means "ONE WAY SAMPLE DATA RECEIVE".

Then 'FORWARD' button is pressed, LCD shows "Sample Data Rcv". It means "HANDSHAKE SAMPLE DATA RECEIVE".

When 'BACKWARD' button is pressed, it changes reversely.

All exclusive communications are based on following structure (Roland Exclusive Format Type IV).

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel # Model-ID # (8-10, MKS-100)
d 0001 0000	Command-ID #
e 0001 0001	Address MSB [] depend on Command-ID
f 0bbb bbbb	Address
g 0ccc cccc	Address LSB
h 0ddd dddd	Data
i 0eee eeee	[]
j 0fff ffff	Checksum
k 1111 0111	End of System Exclusive
Summed value of the all bytes between Command-ID and BOX must be 00H (7 bits). It is not include Command-ID and BOX.	

4. EXCLUSIVE COMMUNICATIONS IN NORMAL MODE

4.1 Communication format

4.1.1 Request (One way) RQ1 11H
(Recognized only)

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel # Model-ID # (8-10, MKS-100)
d 0001 0000	Command-ID # (RQ1)
e 0001 0001	Address MSB
f 0aaa aaaa	Address
g 0bbb bbbb	Address
h 0ccc cccc	Address LSB
i 0ddd dddd	Data
j 0eee eeee	Checksum
k 1111 0111	End of System Exclusive

4.1.2 Data set (One way) DT1 12H
(Transmitted and recognized)

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device ID # = MIDI basic channel where nnnn + 1 = channel # Model-ID # (8-10, MKS-100)
d 0001 0000	Command-ID # (DT1)
e 0001 0010	Address MSB
f 0aaa aaaa	Address
g 0bbb bbbb	Address
h 0ccc cccc	Address LSB
i 0ddd dddd	Data
j 0eee eeee	Checksum
k 1111 0111	End of System Exclusive

Notes :

*4-1 If aaaaaa - cccccc doesn't indicate the top address of the parameter, the message will be ignored.

*4-2 The data size is always ignored and regarded as the size of a parameter which is addressed by aaaaaa - cccccc.

*4-3 Data of one parameter is sent at one time.
Data of only one parameter is recognized at one time.

5. Address mapping of parameters

Address of parameter

000000	Temporary wave parameter block-1	*5-1
0	0aaa aaaa : TONE NAME (ASCII) 9 bytes	*5-2
9	0aaa aaaa : REC KEY 24 - 103	
0A	0aaa aaaa : BANK TUNE 14 - 64 - 114 (-50 - 0 - +50)	
0B	0aaa aaaa : LOOP TUNE 14 - 64 - 114 (-50 - 0 - +50)	
0C	0000 00aa : SCAN MODE 00 : FWD 01 : ALT 10 : BWD	
0D	0000 00aa : LOOP TYPE 00 : 1SHOT 01 : MAN 10 : AUTO	
0E	0000 aaaa : ST (start address)	
	0000 bbbb : ee ddddoccc bbbbaaaa = 0 - NNNNNN	*5-3
	0000 cccc : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
	0000 dddd : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
	0000 00ee : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
13	0000 aaaa : END (end address)	
	0000 bbbb : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
	0000 cccc : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
	0000 dddd : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
	0000 00ee : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
18	0000 aaaa : LP (loop length)	
	0000 bbbb : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
	0000 cccc : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
	0000 dddd : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
	0000 00ee : ee ddddoccc bbbbaaaa = 0 - MNNNNM	*5-3
1D	0000 aaaa : AEN (auto end address)	
	0000 bbbb : ee ddddoccc bbbbaaaa = 4 - MNNNNM	*5-3,4
	0000 cccc : ee ddddoccc bbbbaaaa = 4 - MNNNNM	*5-3,4
	0000 dddd : ee ddddoccc bbbbaaaa = 4 - MNNNNM	*5-3,4
	0000 00ee : ee ddddoccc bbbbaaaa = 4 - MNNNNM	*5-3,4
22	0000 aaaa : ALP (auto loop length)	
	0000 bbbb : ee ddddoccc bbbbaaaa = 4 - MNNNNM	*5-3,4
	0000 cccc : ee ddddoccc bbbbaaaa = 4 - MNNNNM	*5-3,4
	0000 dddd : ee ddddoccc bbbbaaaa = 4 - MNNNNM	*5-3,4
	0000 00ee : ee ddddoccc bbbbaaaa = 4 - MNNNNM	*5-3,4
27	0000 000a : KEY FOLLOW 0 : OFF 1 : ON	
28	0000 000a : PITCH BEND 0 : OFF 1 : ON	
29	0000 000a : VIBRATO 0 : OFF 1 : ON	
2A	0aaa aaaa : ENV V-SRNS 0 - 127	
2B	0aaa aaaa : ENV RATE1 0 - 127	
2C	0aaa aaaa : ENV LEVEL1 0 - 127	
2D	0aaa aaaa : ENV RATE2 0 - 127	
2E	0aaa aaaa : ENV LEVEL2 0 - 127	
2F	0aaa aaaa : ENV RATE3 0 - 127	
30	0aaa aaaa : ENV LEVEL3 0 - 127	
31	0aaa aaaa : ENV RATE4 0 - 127	
32	0aaa aaaa : DYN RANGE 0 - 127	
33	0aaa aaaa : ABEND RATE 0 - 127	
34	0aaa aaaa : ABEND DPTH 0 - 127	
35	0aaa aaaa : SPT KEY#1 24 - 103	
36	0aaa aaaa : SPT KEY#2 24 - 103	*5-5
37	0aaa aaaa : SPT KEY#3 24 - 103	

Temporary wave parameter block-2

37

Temporary wave parameter block-3

37

Temporary wave parameter block-4

37

Performance parameters

0	0aaa aaaa : VIB RATE 0 - 127	
1	0aaa aaaa : M-VIB DPTH 0 - 127	
2	0aaa aaaa : D-VIB DPTH 0 - 127	
3	0aaa aaaa : D-VIB DPTH 0 - 127	
4	0000 000a : BEND MODE 0 : CONT 1 : CHRM	
5	0000 000a : ARP SYNC 0 : INT 1 : EXT	
6	0aaa aaaa : ARP RATE 0 - 127	
7	0000 00aa : ARP MODE 00 : UP 01 : DOWN 10 : U/D 11 : RND	
8	0000 00aa : ARP RANGE 00 : loct 01 : 2oct 10 : 3oct	
9	000a aaaa : ARP REPEAT 1 - 16	
A	0000 aaaa : ARP DECAY 1 - 10	
B	0aaa aaaa : V-MX THRS 0 - 127	
C	0aaa aaaa : V-SW THRS 0 - 127	
D	0000 000a : DTUN MOD 0 : FIX 1 : VELO	
E	0aaa aaaa : DTUN RANGE 0 - 127	
F	0000 000a : ABEND DES 0 : BOTH 1 : HALF	
10	0000 000a : BEND DEST 0 : BOTH 1 : HALF	
11	0aaa aaaa : DELAY TIME 0 - 127	
12	0aaa aaaa : DELAY LEVL 0 - 127	
13	0aaa aaaa : KEY OFFSET 52 - 64 - 76 (-12 - 0 - +12)	
14	0aaa aaaa : TRG G-TIME 0 - 127	
15	0aaa aaaa : TRIGGER KEY #1 23(OFF) - 103	
16	0aaa aaaa : TRIGGER KEY #2 23(OFF) - 103	
17	0aaa aaaa : TRIGGER KEY #3 23(OFF) - 103	
18	0aaa aaaa : TRIGGER KEY #4 23(OFF) - 103	

000900	Structure # of temporary wave parameter blocks	*5-7
0	0000 aaaa : aaaa : structure # of block-1	
	0000 bbbb : bbbb : structure # of block-2	
	0000 cccc : cccc : structure # of block-3	
	0000 dddd : dddd : structure # of block-4	

001000 : 0aaa aaaa : Write command switch

001001 : 0000 000a : ARPEGGIO on/off 0 : OFF
1 : ON

001002 : 0aaa aaaa : Sample dump mode switch

001003 : 0000 00aa : Voice assign mode

0 : MODE-0
1 : MODE-1
2 : MODE-2
3 : MODE-3

Notes :

*5-1 Temporary wave parameters
Transmitted when the parameter (except TONE NAME) is edited or 'Request data' is received.
When 'Data set' command is recognized, the corresponding parameter will be changed.
1-tone uses 1-temporary block, as following chart.
When layer mode (dual-tone, v-mix, v-switch) is selected, 2nd structure (whose LED is "blinking") uses block-2,3.

sampling structure	block # (layer block #)
A	0 (2)
B	0 (2)
C	0 (2)
D	0 (2)
AB	0 (2)
CD	0 (2)
ABCD	0 -
A/B	0/1 (2/3)
C/D	0/1 (2/3)
AB/CD	0/1 -
A/B/C/D	0/1/2/3 -

*5-2 Transmitted only when 'Request data' is received.
If 2 or 4 blocks are used, the top block of them should be used for the communication.

*5-3 These value (NNNNNN, MNNNNM) depends on the sampling structure, as following chart.

structure	NNNNNN	MNNNNM
A	32763 (7FFBH)	32767 (7FFFH)
B	32763 (7FFBH)	32767 (7FFFH)
C	32763 (7FFBH)	32767 (7FFFH)
D	32763 (7FFBH)	32767 (7FFFH)
AB	65531 (FFFBH)	65536 (FFFFH)
CD	65531 (FFFBH)	65536 (FFFFH)
ABCD	131067 (1FFFBH)	131071 (1FFFFH)
A/B	32763 (7FFBH)	32767 (7FFFH)
C/D	32763 (7FFBH)	32767 (7FFFH)
AB/CD	65531 (FFFBH)	65536 (FFFFH)
A/B/C/D	32763 (7FFBH)	32767 (7FFFH)

And the address values must satisfy following conditions.
1: "[start address]+[loop length]" is equal to or less than "[end address]".
2: "[loop length]" is equal to or more than 4.

*5-4 Auto loop addresses are transmitted when it is displayed in edit mode. When Data set command is recognized, the parameter will be changed.

*5-5 If 2 or 4 blocks are used, the SPT KEY # of top block should be used for the communication.
Sampling structure A/B's or C/D's split point is SPT KEY#2.*5-6 Performance parameters
Transmitted when the parameter (except TONE NAME) is edited or 'Request data' is received.
When Data set command (DT1) is recognized, the corresponding parameter will be changed.

*5-7 Structure # of temporary wave parameter
These can't be changed by Data set command (DT1).
Transmitted only when Request data command (RQ1) is received.
If the data of this address is requested to send, structure # of the temporary wave parameter block-n will be transmitted.
If the block would not be used, structure # is 0FH.

structure #	sampling structure
0	A
1	B
2	C
3	D
4	AB
5	CD
6	ABCD
0FH	Not used

*5-8 Write command switch
Transmitted when 'ENTER' button is pressed.
If any data would be written to this address, write the parameters in temporary area to wave parameter area of the banks on the condition of the sampling structure.
Request data command (RQ1) for this address is ignored.

*5-9 Arpeggio on/off switch
Transmitted when 'ARPEGGIO' button is pressed.
When Data set command (DT1) is recognized, arpeggio will turn to ON or OFF.
Request data command (RQ1) for this address is ignored.

*5-10 Sample dump mode switch
Transmitted when 'F1' and 'MIDI' button are pressed.
If any data is written to this address, the mode will change from NORMAL MODE to SAMPLE DATA DUMP MODE.
The transmitter should wait more than 10ms for changing the mode.
Request data command (RQ1) for this address is ignored.

*5-11 Voice assign mode
Transmitted when the voice assign mode is changed with manual operation on the panel of MKS-100.
When Data set command (DT1) is recognized, the voice assign mode will be changed.
Request data command (RQ1) for this address is ignored.
The operation of changing voice assign mode is as follows.

Assign Mode-0 ... Pressing 'FWD', 'BWD' and 'MODE' button.
Assign Mode-1 ... Pressing 'FWD', 'BWD' and 'STANDBY' button.
Assign Mode-2 ... Pressing 'FWD', 'BWD' and 'START' button.
Assign Mode-3 ... Pressing 'F1' and 'F2' button in Assign Mode-1.

6. TRANSMITTED EXCLUSIVE MESSAGES IN SAMPLE DATA DUMP MODE

Sample data is determined by sampling structure.
It is transmitted in following order.

WAVE DATA - WAVE PARAMETER - PERFORMANCE PARAMETER

6.1 One way transfer

6.1.1 Data set DT1 12H

Transmitted when 'ENTER' button is pressed in 'Sample Data Xst' mode.

Byte	Description
1111 0000	Exclusive status
0100 0001	Roland ID #
0000 nnnn	Device-ID # = MIDI basic channel where nnnn + 1 = channel #

d 0001 0000 Model-ID # (S-10, MKS-100)
 e 0001 0010 Command-ID # (DT1)
 f 0aaa aaaa Address MSB
 g 0bbb bbbb Address
 h 0ccc cccc Address LSB
 i 0ddd dddd Data
 j 0eee eeee Checksum
 k 1111 0111 End of System Exclusive

6.2 Handshaking communication

6.2.1 Want to send data WSD 40H

Transmitted when 'ENTER' button is pressed
 in 'Sample Data Xmt.' mode.

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 0000	Model-ID # (S-10, MKS-100)
f 0aaa aaaa	Command-ID # (WSD)
g 0bbb bbbb	Address MSB
h 0ccc cccc	Address
i 0ddd dddd	Address LSB
j 0eee eeee	Size MSB
k 0fff ffff	Size LSB
l 0ggg gggg	Checksum
m 1111 0111	End of System Exclusive

6.2.2 Request data RQD 41H

Transmitted when 'ENTER' button is pressed
 in 'Sample Data Rcv.' mode.

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 0001	Model-ID # (S-10, MKS-100)
f 0aaa aaaa	Command-ID # (RQD)
g 0bbb bbbb	Address MSB
h 0ccc cccc	Address
i 0ddd dddd	Address LSB
j 0eee eeee	Size MSB
k 0fff ffff	Size LSB
l 0ggg gggg	Checksum
m 1111 0111	End of System Exclusive

6.2.3 Data set DAT 42H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 0010	Model-ID # (S-10, MKS-100)
f 0aaa aaaa	Command-ID # (DAT)
g 0bbb bbbb	Address MSB
h 0ccc cccc	Address
i 0ddd dddd	Address LSB
j 0eee eeee	Size MSB
k 0fff ffff	Size LSB
l 0ggg gggg	Checksum
m 1111 0111	End of System Exclusive

6.2.4 Acknowledge ACK 43H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 0011	Model-ID # (S-10, MKS-100)
f 1111 0111	Command-ID # (ACK)

6.2.5 End of data EOD 45H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 0101	Model-ID # (S-10, MKS-100)
f 1111 0111	Command-ID # (EOD)

6.2.6 Communication error ERR 4EH

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 1110	Model-ID # (S-10, MKS-100)
f 1111 0111	Command-ID # (ERR)

6.2.7 Rejection RJC 4FH

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 1111	Model-ID # (S-10, MKS-100)
f 1111 0111	Command-ID # (RJC)

Notes :

*6-1 Address is determined by sampling structure.

Address of first Data set command (DT1, DAT), Want to send data (WSD) or Request data (RQD) is as follows.

structure	WAVE DATA	WAVE PARAMETER	PERFORMANCE PARAMETER
A	020000	010000	010800
B	060000	:	:
C	0A0000	:	:
D	0E0000	:	:
AB	020000	:	:
CD	0A0000	:	:
ABCD	020000	:	:
A/B	020000	:	:
C/D	0A0000	:	:
AB/CD	020000	:	:
A/B/C/D	020000	010000	010800

*6-2 Number of data in one Data set command (DT1) is as follows.

structure	WAVE DATA	WAVE PARAMETER	PERFORMANCE PARAMETER
A	128	73	40
B	:	:	:
C	:	:	:
D	:	:	:
AB	:	:	:
CD	:	:	:
ABCD	:	73	:
A/B	:	146	:
C/D	:	:	:
AB/CD	:	:	:
A/B/C/D	128	146	40

*6-3 Size (MSB - LSB) is as follows.

structure	WAVE DATA	WAVE PARAMETER	PERFORMANCE PARAMETER
A	040000	000049	000028
B	:	:	:
C	:	:	:
D	040000	:	:
AB	080000	:	:
CD	080000	:	:
ABCD	100000	000049	:
A/B	080000	000112	:
C/D	080000	:	:
AB/CD	100000	000112	:
A/B/C/D	100000	000224	000028

7. RECOGNIZED EXCLUSIVE MESSAGES IN SAMPLE DATA DUMP MODE

Transmitted Sample data is determined by sampling structure.
 It must be transmitted in following order.
 WAVE DATA - WAVE PARAMETER - PERFORMANCE PARAMETER

*Following exclusive message is recognized only in
 SAMPLE DATA DUMP MODE.
 When all sample data is received completely,
 sampling structure changes accordingly.

7.1 One way receive

DT1 12H	Byte	Description
a 1111 0000	Exclusive status	
b 0100 0001	Roland ID #	
c 0000 nnnn	Device-ID # = MIDI basic channel	
d 0001 0000	where nnnn + 1 = channel #	
e 0001 0010	Model-ID # (S-10, MKS-100)	
f 0aaa aaaa	Command-ID # (DT1)	
g 0bbb bbbb	Address MSB	
h 0ccc cccc	Address	
i 0ddd dddd	Address LSB	
j 0eee eeee	Size MSB	
k 1111 0111	Size LSB	
l 0ggg gggg	Checksum	
m 1111 0111	End of System Exclusive	

7.2 Handshaking communication

7.2.1 Want to send data WSD 40H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 0000	Model-ID # (S-10, MKS-100)
f 0aaa aaaa	Command-ID # (WSD)
g 0bbb bbbb	Address MSB
h 0ccc cccc	Address
i 0ddd dddd	Address LSB
j 0eee eeee	Size MSB
k 0fff ffff	Size LSB
l 0ggg gggg	Checksum
m 1111 0111	End of System Exclusive

7.2.2 Request data RQD 41H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 0001	Model-ID # (S-10, MKS-100)
f 0aaa aaaa	Command-ID # (RQD)
g 0bbb bbbb	Address MSB
h 0ccc cccc	Address
i 0ddd dddd	Address LSB
j 0eee eeee	Size MSB
k 0fff ffff	Size LSB
l 0ggg gggg	Checksum
m 1111 0111	End of System Exclusive

7.2.3 Data set DAT 42H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 0010	Model-ID # (S-10, MKS-100)
f 0aaa aaaa	Command-ID # (DAT)
g 0bbb bbbb	Address MSB
h 0ccc cccc	Address
i 0ddd dddd	Address LSB
j 0eee eeee	Size MSB
k 0fff ffff	Size LSB
l 0ggg gggg	Checksum
m 1111 0111	End of System Exclusive

7.2.4 Acknowledge ACK 43H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 0011	Model-ID # (S-10, MKS-100)
f 1111 0111	Command-ID # (ACK)

7.2.5 End of data EOD 45H

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 0101	Model-ID # (S-10, MKS-100)
f 1111 0111	Command-ID # (EOD)

7.2.6 Communication error ERR 4EH

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 1110	Model-ID # (S-10, MKS-100)
f 1111 0111	Command-ID # (ERR)

7.2.7 Rejection RJC 4FH

Byte	Description
a 1111 0000	Exclusive status
b 0100 0001	Roland ID #
c 0000 nnnn	Device-ID # = MIDI basic channel
d 0001 0000	where nnnn + 1 = channel #
e 0100 1111	Model-ID # (S-10, MKS-100)
f 1111 0111	Command-ID # (RJC)

Notes :

*7-1 Address of first Data set command (DT1, DAT), Want to send data (WSD) or Request data (RQD) is as follows.

structure	WAVE DATA	WAVE PARAMETER	PERFORMANCE PARAMETER
A	020000	010000	010800
B	060000	:	:
C	0A0000	:	:
D	0E0000	:	:
AB	020000	:	:
CD	0A0000	:	:
ABCD	020000	:	:
A/B	020000	:	:
C/D	0A0000	:	:
AB/CD	020000	:	:
A/B/C/D	020000	010000	010800

*7-2 Number of data in data set is as follows.

structure	WAVE DATA	WAVE PARAMETER	PERFORMANCE PARAMETER
A	2 - 244	73	40
B	:	:	:
C	:	:	:
D	:	:	:
AB	:	:	:
CD	:	:	:
ABCD	:	73	:
A/B	:	146	:
C/D	:	:	:
AB/CD	:	:	:
A/B/C/D	2 - 244	146	40

Number of data of WAVE DATA must be even.

*7-3 Size (MSB - LSB) is as follows.

structure	WAVE DATA	WAVE PARAMETER	PERFORMANCE PARAMETER
A	040000	000049	000028
B	:	:	:
C	:	:	:
D	040000	:	:
AB	080000	:	:
CD	080000	:	:
ABCD	100000	000049	:
A/B	080000	000112	:
C/D	080000	:	:
AB/CD	100000	000112	:
A/B/C/D	100000	000224	000028

8. Address mapping of SAMPLE DATA

Address	Wave parameter of block-1
010000	0aaa aaaa : TONE NAME
9 : 0000 aaaa	SAMPLING STRUCTURE
A : 0000 aaaa	DESTINATION BANK
B : 0000 abcd	a BENDER
	0 : OFF
	1 : ON
	b KEY FOLLOW
	0 : OFF
	1 : ON
	c VIBRATO
	0 : OFF
	1 : ON
	d SAMPLING RATE
	0 : 30 kHz
	1 : 15 kHz
C : 0000 aabb	aa LOOP MODE
	00 : 1SHOT
	01 : MAN
	10 : AUTO
	bb SCAN MODE
	00 : FORWARD
	01 : ALTERNATE
	10 : BACKWARD
D : 0000 aaaa	bbbb aaaa REC KEY NUMBER
E : 0000 bbbb	

Address	Wave parameter of block-1
F : 0000 0000	dummy
10 : 0000 0000	dummy
11 : 0000 aaaa	
12 : 0000 bbbb	
13 : 0000 cccc	
14 : 0000 dddd	
15 : 0000 eeee	
16 : 0000 ffff	
17 : 0000 gggg	
18 : 0000 hhhh	
19 : 0000 iiii	
1A : 0000 jjjj	
1B : 0000 kkkk	
1C : 0000 llll	
1D : 0000 mmmm	
1E : 0000 nnnn	
1F : 0000 oooo	
20 : 0000 pppp	
21 : 0000 qqqq	
22 : 0000 rrrr	
23 : 0000 ssss	

Address	Wave parameter of block-1
24 : 0000 tttt	
25 : 0000 uuuu	
26 : 0000 vvvv	
27 : 0000 wwww	
28 : 0000 xxyy	dummy
uv bbbbaaaa ddddoooo	START ADDRESS
uu ffffeeee hhhggggg	MANUAL LOOP LENGTH
vv jjjjjjjj llllkkkk	MANUAL END ADDRESS
xx nnnnnmmm ppppoooo	AUTO LOOP LENGTH
yy rrrrrqqq tttttsss	AUTO END ADDRESS

Address	Wave parameter of block-1
29 : 0000 aaaa	
2A : 0000 bbbb	bbbbaaaa BANK TUNE
2B : 0000 aaaa	
2C : 0000 bbbb	bbbbaaaa LOOP TUNE
2D : 0000 aaaa	
2E : 0000 bbbb	bbbbaaaa VELOCITY SENSE
2F : 0000 aaaa	
30 : 0000 bbbb	bbbbaaaa ENVELOPE RATE-1
31 : 0000 aaaa	
32 : 0000 bbbb	bbbbaaaa ENVELOPE RATE-2
33 : 0000 aaaa	
34 : 0000 bbbb	bbbbaaaa ENVELOPE RATE-3
35 : 0000 aaaa	
36 : 0000 bbbb	bbbbaaaa ENVELOPE RATE-4
37 : 0000 aaaa	
38 : 0000 bbbb	bbbbaaaa ENVELOPE LEVEL-1
39 : 0000 aaaa	
3A : 0000 bbbb	bbbbaaaa ENVELOPE LEVEL-2
3B : 0000 aaaa	
3C : 0000 bbbb	bbbbaaaa ENVELOPE LEVEL-3
3D : 0000 aaaa	
3E : 0000 bbbb	bbbbaaaa KEY SPLIT POINT-1
3F : 0000 aaaa	
40 : 0000 bbbb	bbbbaaaa KEY SPLIT POINT-2
41 : 0000 aaaa	
42 : 0000 bbbb	bbbbaaaa KEY SPLIT POINT-3
43 : 0000 aaaa	
44 : 0000 bbbb	bbbbaaaa DYNAMIC SENS
45 : 0000 aaaa	
46 : 0000 bbbb	bbbbaaaa AUTO BEND RATE
47 : 0000 aaaa	
48 : 0000 bbbb	bbbbaaaa AUTO BEND DEPTH

Address	Wave parameter of block-1
010049	Wave parameter of block-2
010111	
010112	Wave parameter of block-3
01015A	
01015B	Wave parameter of block-4
010224	
010800	Performance parameter


```
26 : 0000 abcd :
a AUTO BEND DESTINATION OF DETUNE MODE
0 : BOTH
1 : HALF
b BEND DESTINATION OF DETUNE MODE
0 : BOTH
1 : HALF
c BENDER MODE
0 : CONTINUOUS
1 : CHROMATIC
d DETUNE MODE
0 : FIX
1 : VELOCITY
```

```
27 : 0000 0000 : dummy
020000 : Wave data of bank-1
0 : 0aaa aaaa :
1 : 0bbb bb00 :
aaaa aaabbbb Wave data
(12 bit 2's complement)
057F7F :
060000 : Wave data of bank-2
097F7F :
0A0000 : Wave data of bank-3
0D7F7F :
0E0000 : Wave data of bank-4
127F7F :
```

9. Sequence of communication

9.1 When one way data set of WAVE DATA is transmitted

```
this unit      message      objective unit
-----
DTI(WAVE DATA) ----->
* time interval about 20 ms
DTI(WAVE DATA) ----->
:
DTI(WAVE DATA) ----->
DTI(WAVE PARAMETER) ----->
[ DTI(WAVE PARAMETER) -----> ]
DTI(PERFORMANCE PARAMETER) ----->
```

9.2 When one way data set of WAVE DATA is received

```
this unit      message      objective unit
-----
<----- DTI(WAVE DATA)
* wait time more than 20 ms
<----- DTI(WAVE DATA)
:
<----- DTI(WAVE DATA)
<----- DTI(WAVE PARAMETER)
[ <----- DTI(WAVE PARAMETER) ]
<----- DTI(PERFORMANCE PARAMETER)
```

9.3 When want to send data is received

```
this unit      message      objective unit
-----
<----- WSD(WAVE DATA)
ACK ----->
<----- DAT(WAVE DATA)
ACK ----->
:
<----- DAT(WAVE DATA)
ACK ----->
<----- EOD
ACK ----->
<----- WSD(WAVE PARAMETER)
ACK ----->
<----- DAT(WAVE PARAMETER)
ACK ----->
[ <----- DAT(WAVE PARAMETER) ]
[ ACK -----> ]
<----- EOD
ACK ----->
<----- WSP(PERFORMANCE PARAMETER)
ACK ----->
<----- DAT(PERFORMANCE PARAMETER)
ACK ----->
<----- EOD
ACK ----->
```

9.4 When request data is received

```
this unit      message      objective unit
-----
<----- RQD(WAVE DATA)
DAT(WAVE DATA) ----->
<----- ACK
:
DAT(WAVE DATA) ----->
<----- ACK
EOD ----->
<----- ACK
<----- RQD(WAVE PARAMETER)
DAT(WAVE PARAMETER) ----->
<----- ACK
[ DAT(WAVE PARAMETER) -----> ]
[ <----- ACK ]
```

```
EOD ----->
<----- ACK
<----- RQD(PERFORMANCE PARAMETER)
DAT(PERFORMANCE PARAMETER) ----->
<----- ACK
EOD ----->
<----- ACK
```

Notes :

- *When it receives ERR, it sends same data set again.
- *When a transmitting MKS-100 receives any illegal command (ie. a note on etc.), it ignores and waits for legal command.
- *When a receiving MKS-100 receives any illegal command (ie. a note on etc.), it ignores and waits for legal command.
- *It sends RJC and stops sample dump sequence immediately, when sampling structure button is pressed.
- *It stops the sequence immediately when it receives RJC.

8-voice digitai sampling module

MODEL MKS-100 MIDI Implementation Chart

Date: Oct. 18 1986
Version: 1.00

Function.....		Transmitted	Recognized	Remarks
Basic Channel	Default Changed	1-16 1-16	1-16 1-16	Memorized
Mode	Default Messages Altered	× × *****	Mode 3, 4 Poly, Mono	Memorized Omni on, off ignored
Note Number	True voice	× *****	24-103 24-103	Depends on Key Range
Velocity	Note ON Note OFF	× ×	○ v=1-127 ×	
After Touch	Key's Ch's	× ×	× ×	
Pitch Bender		×	*1 0-12 semi-tone	9 bit resolution
Control Change	1 64 100,101 6,38	× × *1, *2 (0, 1) *1, *2	*1 *1 *1, *2 (0, 1) *1, *2	Modulation Hold 1 RPC LSB, MSB Data Entry MSB, LSB
Prog Change	True #	*1 0-122 *****	*1 0-127 0-127	
System Exclusive		*1	*1	
System Common	Song Pos Song Sel Tune	× × ×	× × ×	
System Real Time	Clock Commands	× ×	× ×	
Aux Mes-sages	Local ON/OFF All Notes OFF Active Sense Reset	× × × ×	× ○ (123-127) ○ ×	
Notes	*1 Can be set to ○ or × manually, and memorized. RPC=Registered parameter control number. RPC #0 : Pitch bend sensitivity RPC #1 : Master fine tuning Parameter values are given by Data Entry.			

Mode 1 : OMNI ON, POLY
Mode 3 : OMNI OFF, POLY

Mode 2 : OMNI ON, MONO
Mode 4 : OMNI OFF, MONO

○ : Yes
× : No