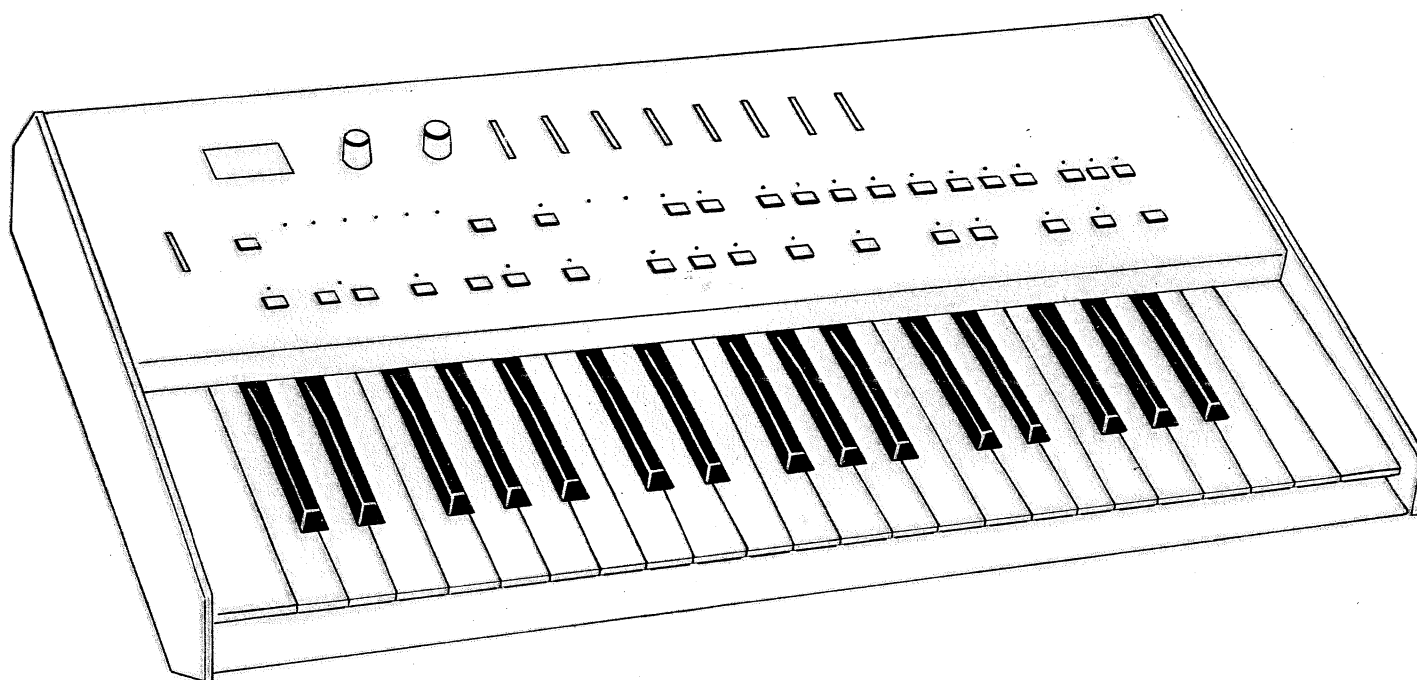




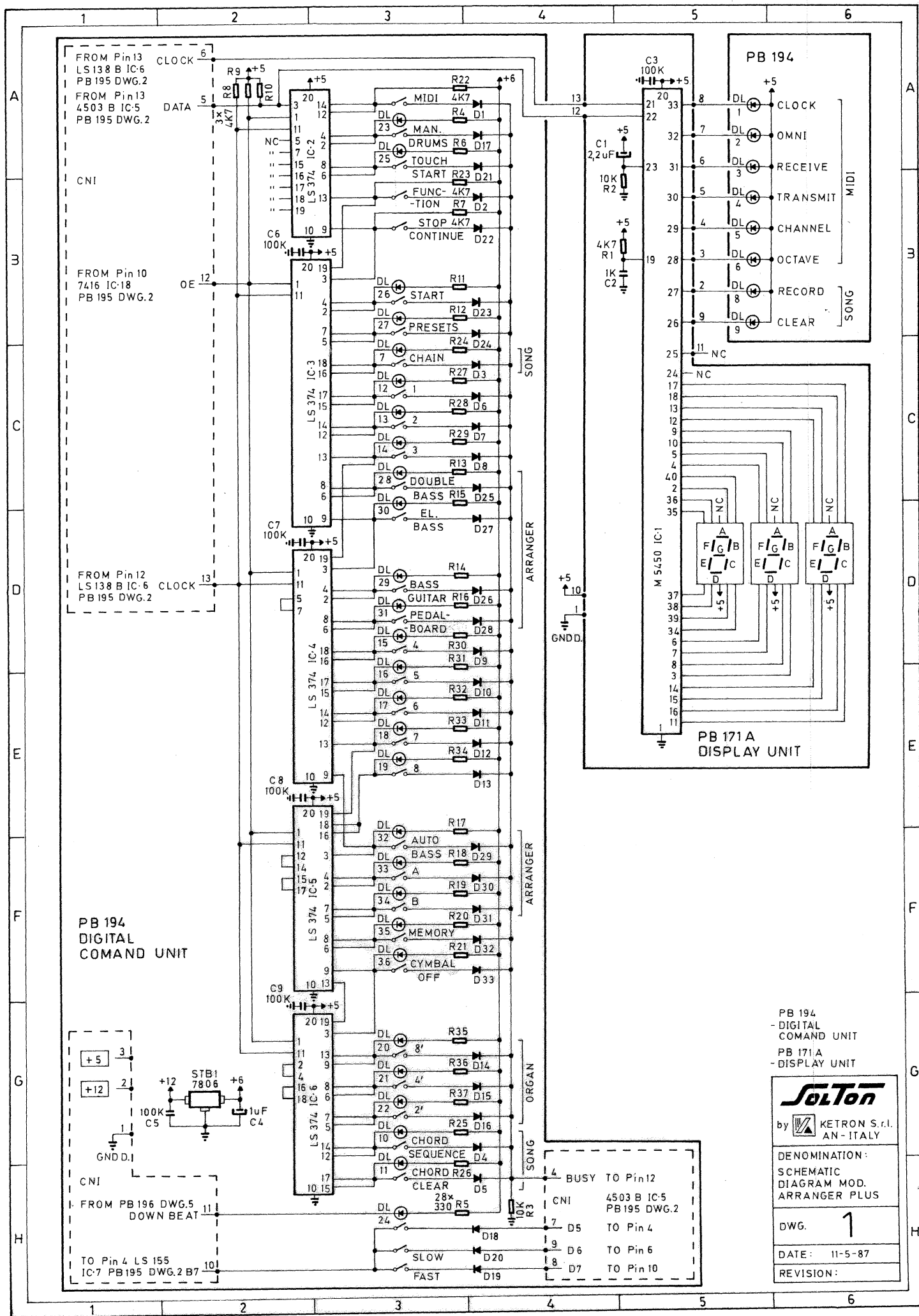
SCHEMATIC DIAGRAM
Mod. ARRANGER PLUS

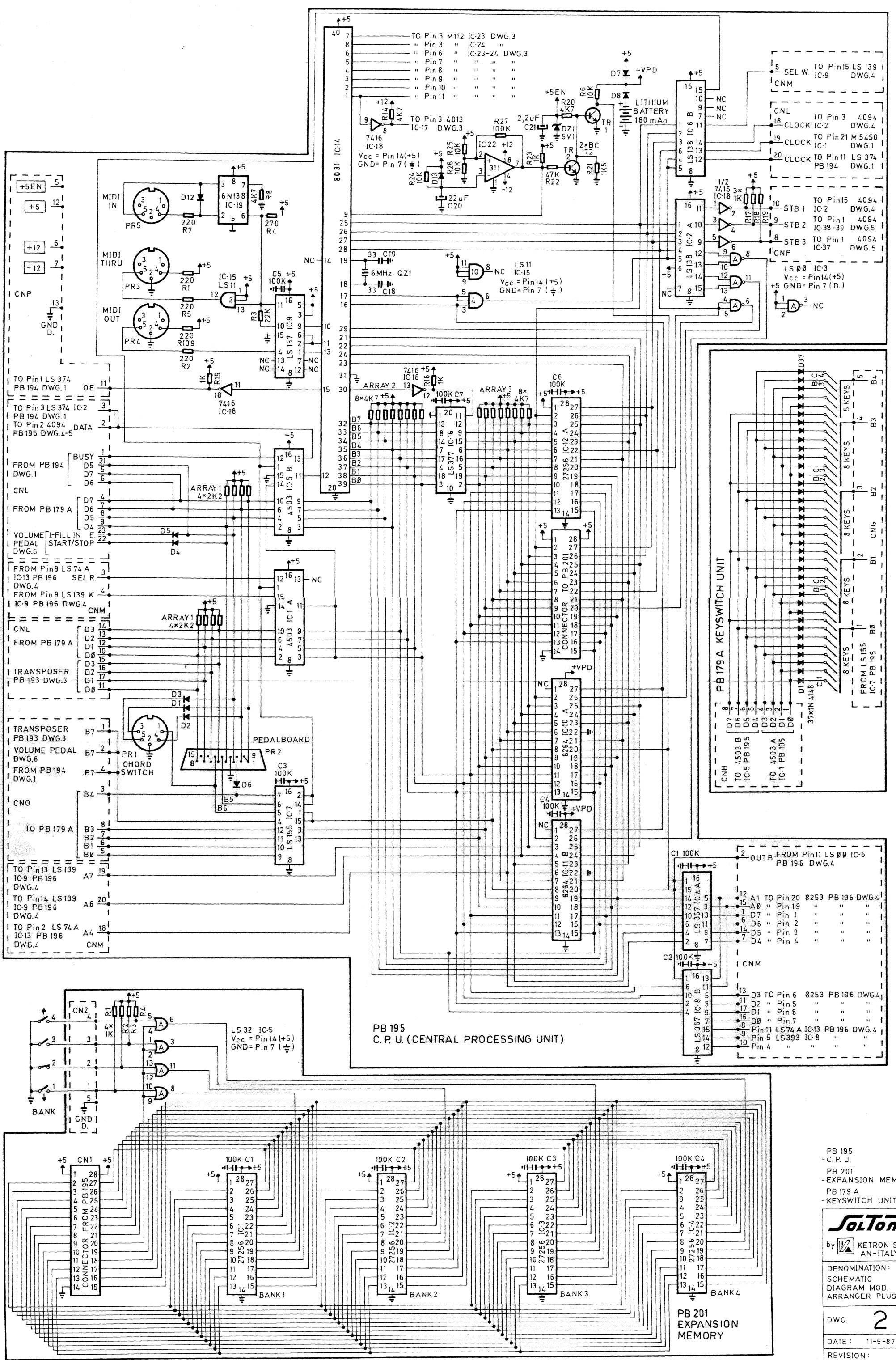
A PRODUCT MADE IN ITALY BY:

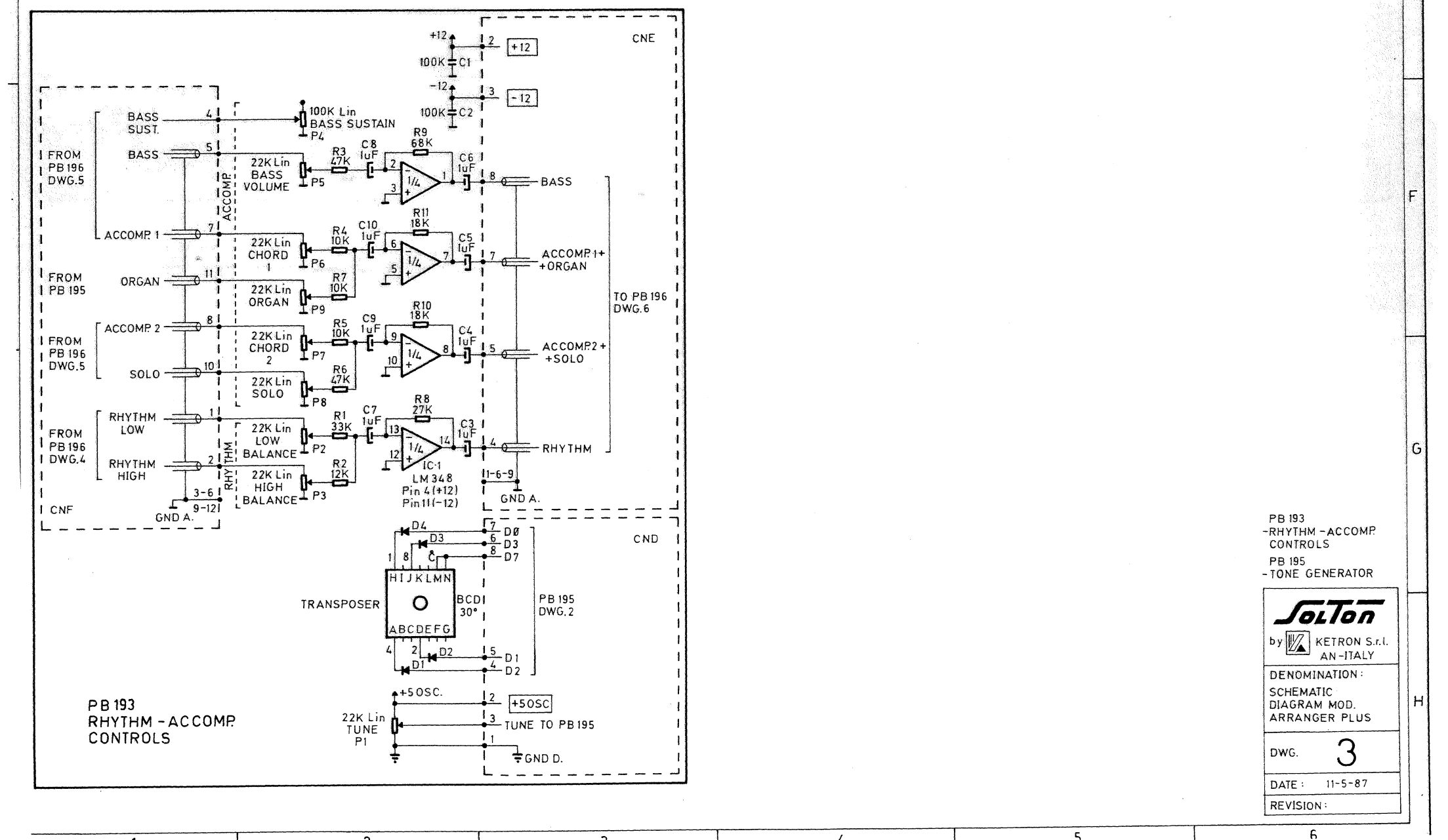
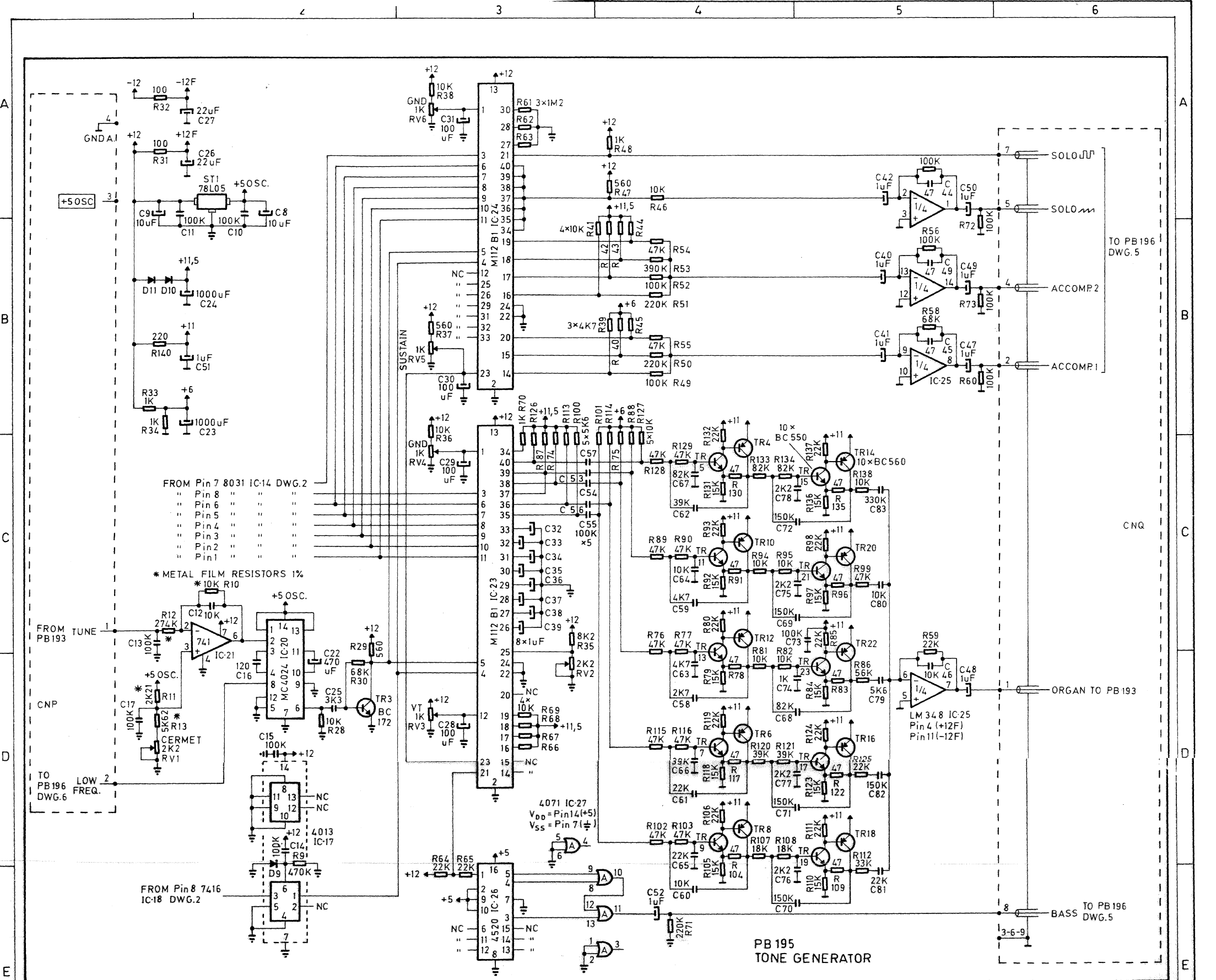


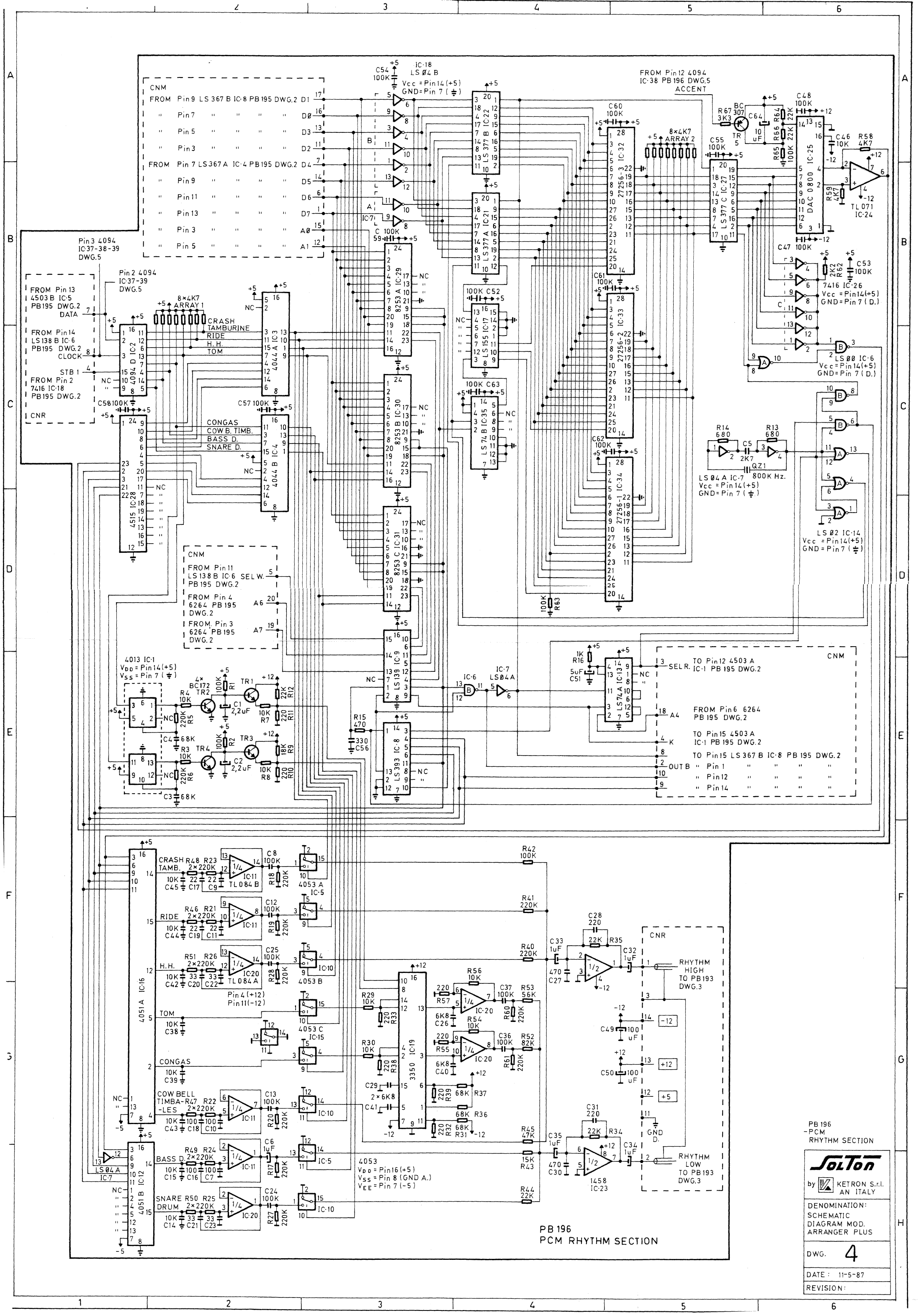
S.r.l.

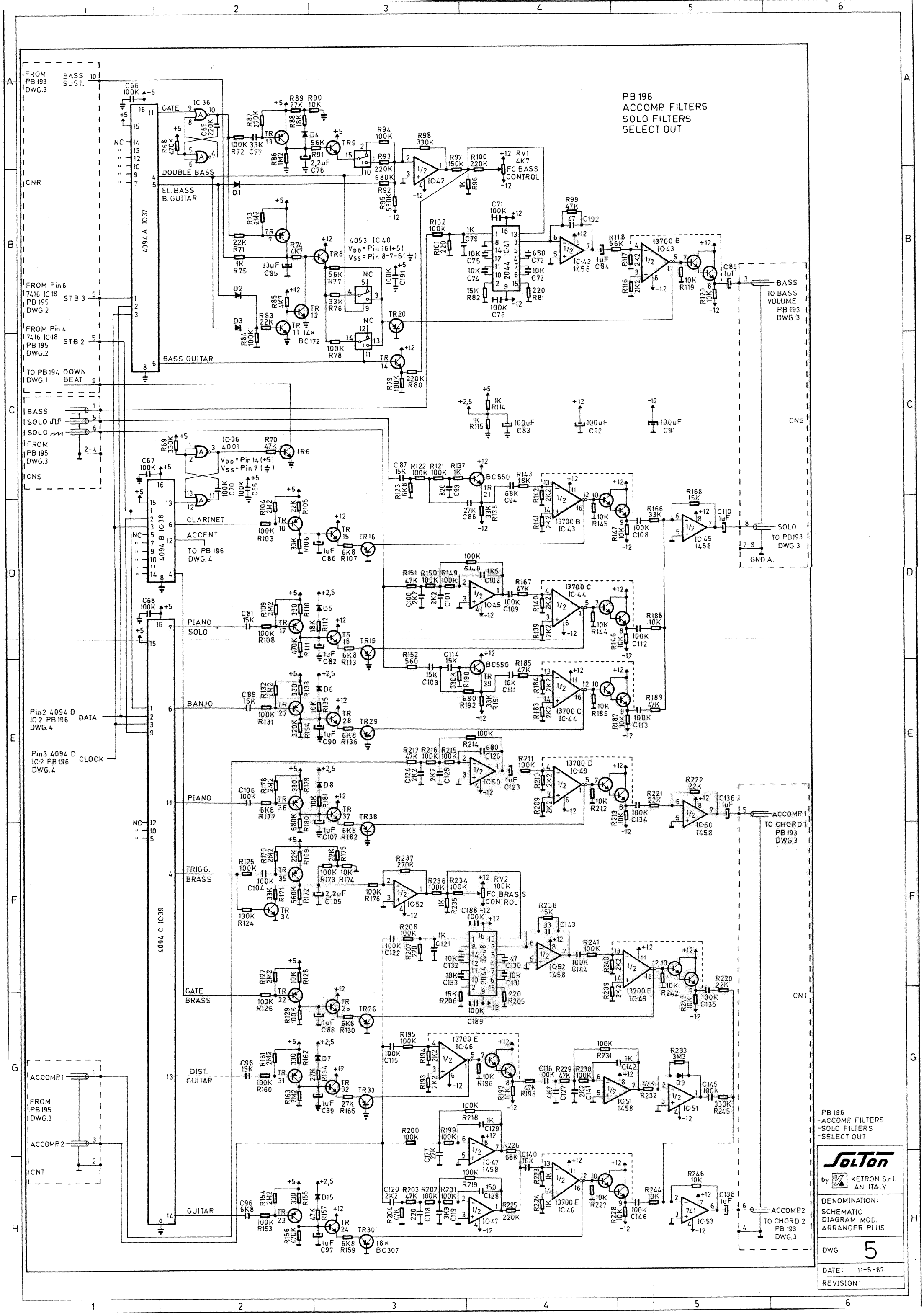
VIA G. DI VITTORIO 13
60020 CANDIA-ANCONA
tel. 071-8046059
ITALY

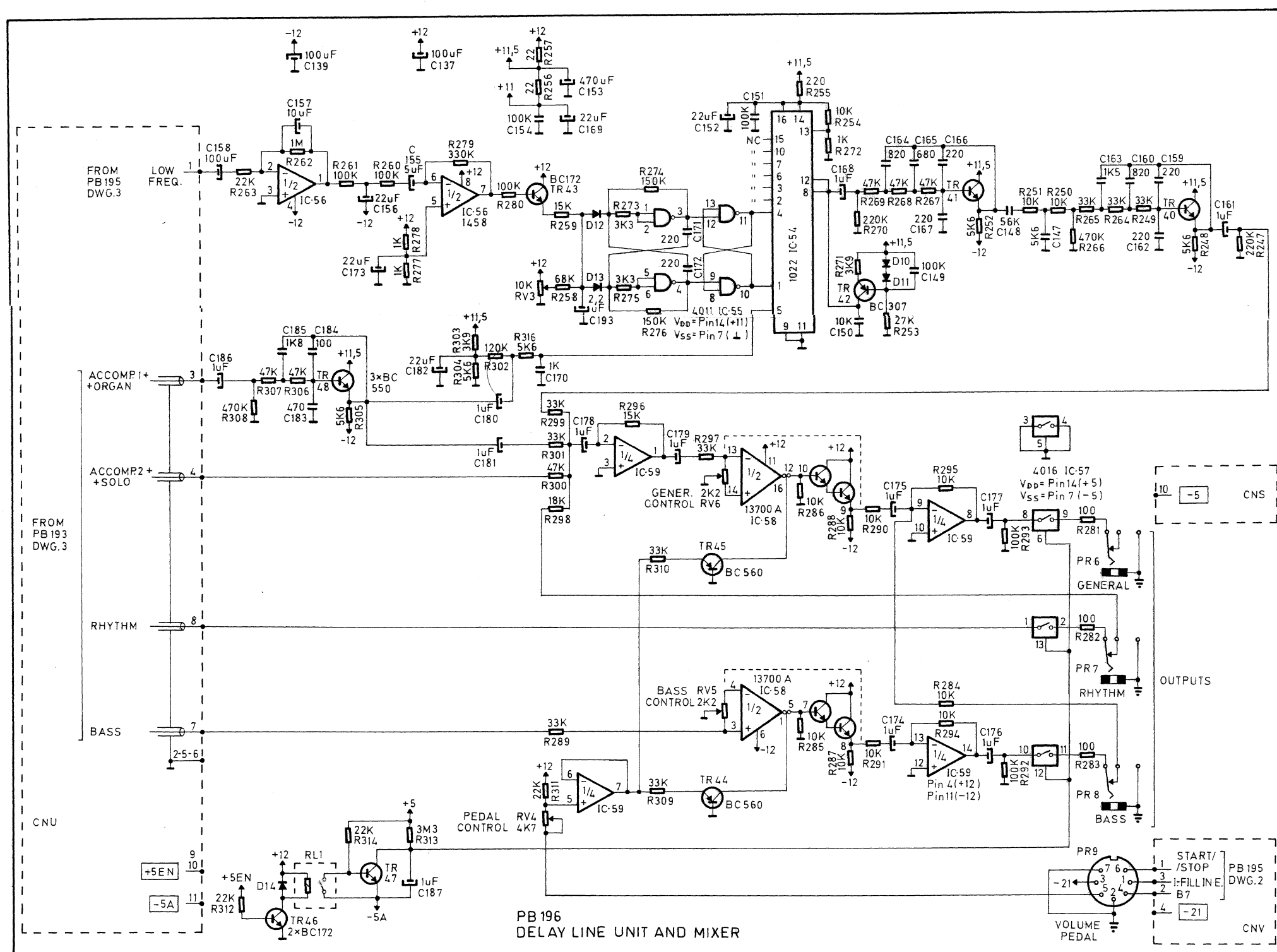
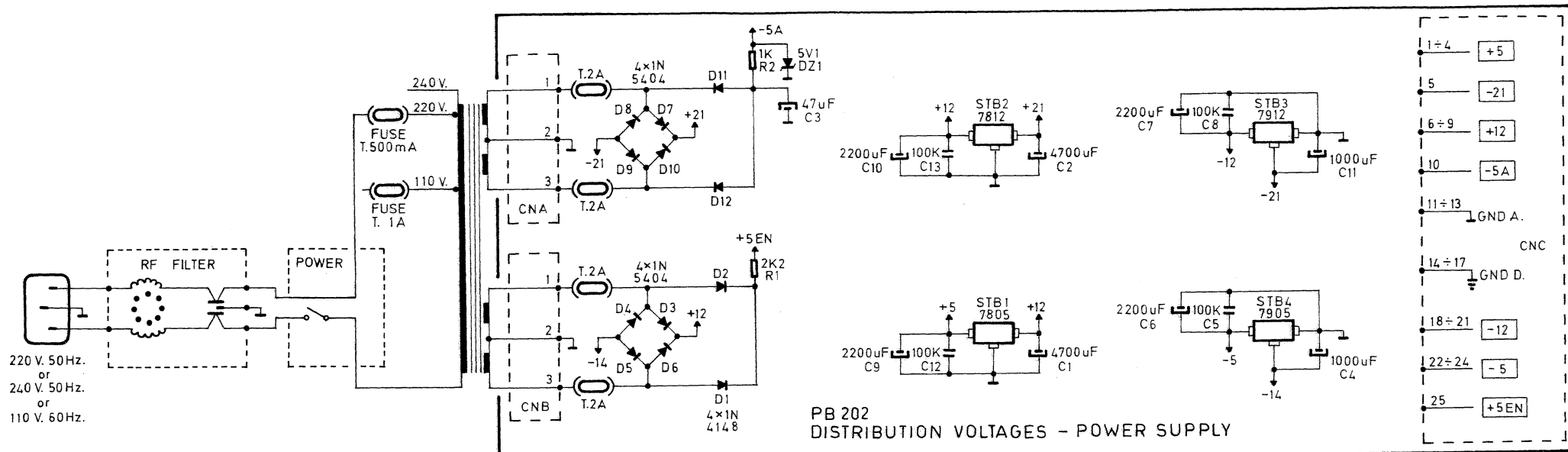












PB 202
- DISTRIBUTION VOLTAGES
POWER SUPPLY
PB 196
- STRING UNIT-MIXER

SolTon
by KETRON S.r.l.
AN-ITALY

DENOMINATION:
SCHEMATIC
DIAGRAM MOD.
ARRANGER PLUS

DWG. 6

DATE: 11-5-87

REVISION:

Vss	1	40	OUT BIT 18
OUT BIT 17	2	39	" " 19
" " 16	3	38	" " 20
" " 15	4	37	" " 21
" " 14	5	36	" " 22
" " 13	6	35	" " 23
" " 12	7	34	" " 24
" " 11	8	33	" " 25
" " 10	9	32	" " 26
" " 9	10	31	" " 27
" " 8	11	30	" " 28
" " 7	12	29	" " 29
" " 6	13	28	" " 30
" " 5	14	27	" " 31
" " 4	15	26	" " 32
" " 3	16	25	" " 33
" " 2	17	24	" " 34
" " 1	18	23	DATA ENABLE
BRIGHTNESS CONTROL	19	22	DATA IN
Vdd	20	21	CLOCK IN

P1.0	1	40	Vcc
P1.1	2	39	P0.0 AD0
P1.2	3	38	P0.1 AD1
P1.3	4	37	P0.2 AD2
P1.4	5	36	P0.3 AD3
P1.5	6	35	P0.4 AD4
P1.6	7	34	P0.5 AD5
P1.7	8	33	P0.6 AD6
RST/VPD	9	32	P0.7 AD7
RXD P3.0	10	31	EA
TXD P3.1	11	30	ALE
INT0 P3.2	12	29	PSEN
INT1 P3.3	13	28	P2.7 A15
T0 P3.4	14	27	P2.6 A14
T1 P3.5	15	26	P2.5 A13
WR P3.6	16	25	P2.4 A12
RD P3.7	17	24	P2.3 A11
XTAL 1	18	23	P2.2 A10
XTAL 2	19	22	P2.1 A9
Vss	20	21	P2.0 A8

ANALOG GROUND VSA	1	40	O1E
Vss	2	39	O5E
STROBE STD	3	38	O4E OCTAVE
RESET	4	37	O6E OUTPUTS
CLOCK	5	36	O2E
D1	6	35	O3E
D2	7	34	O7E
D3	8	33	CH5
D4	9	32	CH6
D5	10	31	CH7
D6	11	30	CH4
ADR CONTROL -VT	12	29	CH8
Vdd	13	28	CH3
FM1	14	27	CH2
FM2	15	26	CH1
FM2E	16	25	VAR-ANALOG RELEASE
FM1E	17	24	Vreg
FH1E	18	23	V SUSTAIN CONTROL
FLE	19	22	PERC M2
FL	20	21	CI m-MONOPHONIC OUT

Vpp	1	28	Vdd
A12	2	27	A14
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE
A2	8	21	A10
A1	9	20	CE
A0	10	19	D7
D0	11	18	D6
D1	12	17	D5
D2	13	16	D4
Vss	14	15	D3

NC	1	28	Vcc
A12	2	27	WE
A7	3	26	CS2
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE
A2	8	21	A10
A1	9	20	CS1
A0	10	19	I/O8
I/O1	11	18	I/O7
I/O2	12	17	I/O6
I/O3	13	16	I/O5
GND	14	15	I/O4

D7	1	24	Vcc
D6	2	23	WR
D5	3	22	RD
D4	4	21	CS
D3	5	20	A1
D2	6	19	A0
D1	7	18	CLK 2
D0	8	17	OUT 2
CLK 0	9	16	GATE 2
OUT 0	10	15	CLK 1
GATE 0	11	14	GATE 1
GND	12	13	OUT 1

THRESHOLD CONTROL V _{LC}	1	16	COMPENSATION
I _{OUT}	2	15	VREF(-)
V-	3	14	VREF(+)
I _{OUT}	4	13	V+
MSB B1	5	12	B8 LSB
B2	6	11	B7
B3	7	10	B6
B4	8	9	B5

I _{REF}	1	16	Vcc
V _{IF}	2	15	VBP
V _{LP}	3	14	V _{IV}
V _{IV}	4	13	V _{LP}
VBP	5	12	V _{IF}
V _{CQ}	6	11	V _{CQ}
V _{EE}	7	10	V _{CF}
V _{CF}	8	9	GND

SIG IN+	1	16	+V
Q CONTROL	2	15	SIG IN -
OUT	3	14	C1A
C4A	4	13	FREQ. CONTROL
C4B	5	12	C1B
C3A	6	11	C2A
C3B	7	10	C2B
GND	8	9	-V

CLOCK INPUT 1	1	16	GROUND
NC	2	15	NC
NC	3	14	NC
CLOCK INPUT 2	4	13	TETRODE GATE
SIGNAL INPUT	5	12	OUTPUT 512
NC	6	11	NC
NC	7	10	NC
OUTPUT 513	8	9	NEGATIVE SUPPLY

NC	1	8	Vcc
ANODE	2	7	V _b
CATHODE	3	6	V ₀
NC	4	5	GND

1 CLR	1	14	Vcc
1D	2	13	2CLR
1CK	3	12	2D
1PR	4	11	2CK
1Q	5	10	2PR
1Q	6	9	2Q
GND	7	8	2Q

SELECT	A	1	16	Vcc
	B	2	15	Y0
	C	3	14	Y1
ENABLE	G2A	4	13	Y2
	G2B	5	12	Y3
	G1	6	11	Y4
OUTPUT Y7	7	10	Y5	
GND	8	9	Y6	

1G ENABLE	1	16	Vcc	
SELECT	1A	2	15	2G ENABLE
	1B	3	14	2A
DATA OUTPUTS	1Y0	4	13	2B
	1Y1	5	12	2Y0
	1Y2	6	11	2Y1
	1Y3	7	10	2Y2
	GND	8	9	2Y3

Ea	1	16	Vcc
Ea	2	15	E _b
A1	3	14	E _b
03a	4	13	A0
02a	5	12	03b
01a	6	11	02b
00a	7	10	01b
GND	8	9	00b

S	1	16	Vcc
I _{0a}	2	15	E
I _{1a}	3	14	I _{0c}
Za	4	13	I _{1c}
I _{0b}	5	12	Zc
I _{1b}	6	11	I _{0d}
Zb	7	10	I _{1d}
GND	8	9	Zd

G1	1	16	Vcc
1A	2	15	G2
1Y	3	14	6A
2A	4	13	6Y
2Y	5	12	5A
3A	6	11	5Y
3Y	7	10	4A
GND	8	9	4Y

OE	1	20	Vcc
O0	2	19	O7
D0	3	18	D7
D1	4	17	D6
O1	5	16	O6
O2	6	15	O5
D2	7	14	D5
D3	8	13	D4
O3	9	12	O4
GND	10	11	CP

E	1	20	Vcc
Q0	2	19	Q7
D0	3	18	D7
D1	4	17	D6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	D5
D3	8	13	D4
Q3	9	12	Q4
GND	10	11	CP

1A	1	14	Vcc
1 CLEAR	2	13	2A
1QA	3	12	2CLEAR
1QB	4	11	2QA
1QC	5	10	2QB
1QD	6	9	2QC
GND	7	8	2QD

Q1	1	14	Vdd
Q1	2	13	Q2
CP1	3	12	Q2
CD1	4	11	CP2
D1	5	10	CD2
SD1	6	9	D2
Vss	7	8	SD2

Vcc (VCM) (13)	1	14	Vcc (OUT BUFFER)
DC CONTROL IN (12)	2	13	NC
C _x L _x 2 (11)	3	12	"
CD1 X1 (10)	4	11	"
GND (VCM) (9)	5	10	"
OUT (8)	6	9	"
GND (OUT BUFFER)	7	8	"

Q3	1	16	Vdd
NC	2	15	S ₃
S ₀	3	14	R ₃
R ₀	4	13	Q ₀
E ₀	5	12	R ₂
R ₁	6	11	S ₂
S ₁	7	10	Q ₂
Vss	8	9	Q ₁

CHANNELS	4	1	16	V _{DD}	
IN/OUT	6	2	15	2	
COM OUT/IN	3	14	1	CHANNELS IN/OUT	
CHANNELS	7	4	13		0
IN/OUT	5	5	12		3
	6	11	A		
INH	7	10	B		
V _{EE}	8	9	C		
V _{SS}					

by	1	16	Vdd
bx	2	15	OUT/IN bx or by
cy	3	14	OUT/IN ax or ay
IN/OUT	4	13	ay
IN/OUT	5	12	ax
INH	6	11	A
V _{EE}	7	10	B
Vss	8	9	C

STROBE	1	16	Vdd
DATA	2	15	OUT ENABLE
CLOCK	3	14	Q5
Q1	4	13	Q6
Q2	5	12	Q7
Q3	6	11	Q8
Q4	7	10	Q _S
Vss	8	9	Q _S

DISABLE A	1	16	Vdd
D1	2	15	DISABLE B
Q1	3	14	D6
D2	4	13	Q6
Q2	5	12	D5
D3	6	11	Q5
Q3	7	10	D4
Vss	8	9	Q4

STROBE	1	24	Vdd
DATA 1	2	23	INHIBIT
DATA 2	3	22	DATA 4
S7	4	21	DATA 3
S6	5	20	S10
S5	6	19	S11
S4	7	18	S8
S3	8	17	S9
S2	9	16	S14
S1	10	15	S15
S0	11	14	S12
Vss	12	13	S13

CLOCK A	1	16	Vdd
ENABLE A	2	15	RESET B
Q1A	3	14	Q4 B
Q2A	4	13	Q3 B
Q3A	5	12	Q2 B
Q4A	6	11	Q1 B
RESET A	7	10	ENABLE B
Vss	8	9	CLOCK B